IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF DELAWARE

SAMSUNG ELECTRONICS CO., LTD. AND SAMSUNG SEMICONDUCTOR, INC. Plaintiffs, v. NETLIST, INC., Defendant.	C.A. No. 21-1453-RGA **Jury Trial Demanded**
NETLIST, INC., Counter-Plaintiff, v. SAMSUNG ELECTRONICS CO., LTD. AND SAMSUNG SEMICONDUCTOR, INC. Counter-Defendants.	
NETLIST, INC. Cross-Plaintiff, v. GOOGLE LLC AND ALPHABET INC. Cross-Defendants.	

DEFENDANT NETLIST, INC.'S FIRST AMENDED ANSWER, AFFIRMATIVE DEFENSES, COUNTERCLAIMS, AND CROSS-CLAIMS TO THE FIRST AMENDED COMPLAINT

On January 18, 2022, plaintiffs Samsung Electronics Co., Ltd. ("SEC") and Samsung Semiconductor, Inc. ("SSI") (collectively "Plaintiffs" or "Samsung") filed the First Amended Complaint for Declaratory Judgment of Non-Infringement and Unenforceability; Breach of Contract ("FAC") against Defendant Netlist, Inc. ("Netlist"). D.I. 14. The FAC seeks a declaration that Samsung does not directly or indirectly infringe United States Patent Nos. 10,217,523 (the "'523 patent"), 10,474,595 (the "'595 patent"), 9,858,218 (the "'218 patent"), 7,619,912 (the "'912 patent"), 10,860,506 (the "'506 patent"), 10,949,339 (the "'339 patent"), and 11,016,918 (the "'918 patent"). *Id*.

On August 1, 2022, this Court entered an order dismissing Count IV (noninfringement of the '912 patent), Count V (noninfringement of the '506 patent), Count VI (noninfringement of the '339 patent), Count VII (noninfringement of the '918 patent), Count X (unenforceability of the '912 patent), and Count XI (unenforceability of the '506 patent) of Plaintiffs' FAC. D.I. 38.

Netlist, by and through its undersigned attorneys, submits this First Amended Answers to the remaining portions of Samsung's FAC. Solely for convenience, some of the headings from the FAC are reproduced here. Any allegations not specifically admitted herein are denied.

Netlist further asserts its First Amended Counterclaims against Samsung and Cross-claims against Google LLC and Alphabet Inc. (together with Google LLC "Google").

NATURE OF THE ACTION

1. Netlist admits that Plaintiffs have filed this lawsuit but denies any liability including for declaratory judgment and breach of contract. Netlist denies that Plaintiffs are entitled to the relief they seek.

2. Netlist admits that Netlist and SEC entered into a Joint Development and License Agreement (the "JDLA") in November 2015, which granted Samsung a license to certain Netlist's

patents subject to various exceptions and limitations. Netlist admits that it has terminated the JDLA no later than July 15, 2020. It is admitted that Netlist asserts that Samsung infringes the Patents-in-Suit. The remaining allegations in this paragraph state legal conclusions to which no response is required. To the extent any response is necessary, Netlist denies.

3. The allegations in this paragraph state a legal conclusion to which no response is required. To the extent any response is necessary, Netlist denies.

THE PARTIES

4. Netlist is without knowledge sufficient to admit or deny the allegations in this paragraph of the Complaint and, therefore, denies.

5. Netlist is without knowledge sufficient to admit or deny the allegations in Paragraph 5 of the Complaint and, therefore, denies.

6. Netlist admits that it has filed a registration for incorporation under the laws of the State of Delaware. With respect to the remaining allegations in paragraph 6, Netlist denies.

JURISDICTION AND VENUE

7. The allegations of Paragraph 7 state a legal conclusion to which no response is required. To the extent further response is necessary, Netlist denies.

8. The allegations of Paragraph 8 state a legal conclusion to which no response is required. To the extent further response is necessary, Netlist denies.

9. Netlist admits that this Court has personal jurisdiction over Netlist.

10. Netlist admits that this Court is a proper venue for this Action.

11. The allegations of Paragraph 11 state a legal conclusion to which no response is required. To the extent further response is necessary, Netlist denies.

12. Paragraph 12 purports to reference a Notice of Infringement letter Netlist sent to SEC and SSI, which speaks for itself. Except as expressly admitted, Netlist denies the allegations of Paragraph 12.

13. Netlist admits that it previously asserted Netlist's U.S. Patent Nos. 9,858,218; 10,474,595; and 10,217,523 patents in litigation against SK hynix, Inc. and SK hynix America Inc. (collectively "SK hynix"). To the extent Plaintiffs contend that Netlist made any specific allegations in a separate action, the pleadings Netlist filed in such an action speak for themselves, and therefore no response is needed. Except as expressly admitted, Netlist denies the allegations of Paragraph 13.

14. Based on the Court's Order dismissing Plaintiffs' claims relating to the '912 patent, D.I. 38, no response is needed to this paragraph. To the extent further response is necessary, Netlist denies as to facts purportedly attributable to Netlist. Netlist is also without knowledge sufficient to admit or deny the allegations attributable to Samsung and third parties, and therefore, denies.

15. Based on the Court's Order dismissing Plaintiffs' claims relating to the '912 patent, D.I. 38, no response is needed to this paragraph. To the extent further response is necessary, Netlist's pleadings in the referenced prior actions speak for themselves.

16. Based on the Court's Order dismissing Plaintiffs' claims relating to the '506, '339, and '918 patents, D.I. 38, no response is needed to this paragraph. To the extent Plaintiffs contend that Netlist made any specific allegations in a separate action, the pleadings and patent documents Netlist filed in such an action speak for themselves. Except as expressly admitted, Netlist denies the allegations of this paragraph.

17. Netlist admits that it is a party to *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 6:21-cv-430 (W.D. Tex.) and *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 6:21-cv-431 (W.D.

Tex.). To the extent Plaintiffs contend that Netlist made any specific allegations in a separate action, the pleadings and patent documents Netlist filed in such an action speak for themselves, and therefore no response is needed. Except as expressly admitted, Netlist denies the allegations of this paragraph.

18. To the extent Plaintiffs contend that Netlist made any specific allegations in a separate action, the pleadings and patent documents Netlist filed in such an action speak for themselves, and therefore no response is needed.

19. Netlist admits that it requested that Samsung take a license, that Samsung is on notice of all of Netlist's patents, and that Samsung declined. Except as expressly admitted, Netlist denies the allegations of this paragraph.

20. The allegations of Paragraph 20 call for a legal conclusion to which no response is required. To the extent any response is necessary, Netlist denies.

BACKGROUND

21. Netlist admits that it entered into the JDLA with SEC on November 12, 2015. To the extent that Plaintiffs state that the JDLA included certain provisions, the JDLA speaks for itself and therefore no response is needed. Except as expressly admitted, Netlist denies the allegations of this paragraph.

22. To the extent that Plaintiffs state that the JDLA included certain provisions, the JDLA speaks for itself and therefore no response is needed. Except as expressly admitted, Netlist denies the allegations of this paragraph.

23. To the extent that Plaintiffs state that the JDLA includes certain provisions, the JDLA speaks for itself and therefore no response is needed. Except as expressly admitted, Netlist denies the allegations of this paragraph.

24. To the extent that Plaintiffs state that the JDLA includes certain provisions, the JDLA speaks for itself and therefore no response is needed. With respect to the remaining allegations in paragraph 24, Netlist denies.

25. Denied.

26. Paragraph 26 purports to reference a letter sent from Mr. Marc J. Frechette to Mr. Seung Min Sung. The referenced letter speaks for itself and therefore no response is needed. With respect to the remaining allegations in paragraph 24, Netlist denies.

27. Netlist admits that on May 28, 2020, the U.S. District Court for the Central District of California docketed Netlist's complaint against SEC, *Netlist Inc v. Samsung Electronics Co., Ltd.,* No. 8:20-cv-00993-MCS (C.D. Cal.) ("Breach Action").

28. Paragraph 28 purports to reference a letter sent from Mr. Marc J. Frechette to Mr. Seung Min Sung. The referenced letter speaks for itself and therefore no response is needed. With respect to the remaining allegations in paragraph 28, Netlist denies.

29. Paragraph 29 purports to reference Netlist's amended complaint filed in the Breach Action and the referenced amended complaint speaks for itself. Except as expressly admitted, Netlist denies the allegations of this paragraph.

30. Paragraph 30 purports to reference a letter sent from Mr. Marc J. Frechette to Mr. Seung Min Sung, and the letter speaks for itself. Except as expressly admitted, Netlist denies the allegations of this paragraph.

31. Paragraph 31 purports to reference a letter from Netlist's outside counsel to SEC dated October 15, 2020. The referenced letter speaks for itself and therefore no response is needed. Except as expressly admitted, Netlist denies the allegations of this paragraph.

32. Paragraph 32 purports to reference an email from Mr. Marc J. Frechette to Samsung. The referenced Email speaks for itself and therefore no response is needed. Except as expressly admitted, Netlist denies the allegations of this paragraph.

33. Denied.

34. Admitted.

35. Netlist admits that a jury trial was held in the action *Netlist Inc. v. Samsung Electronics Co., Ltd*., No. 8:20-cv-993-MCS (C.D. Cal.). Paragraph 35 purports to reference the jury verdict, Samsung's motion, and other briefings and filings in the *Netlist Inc. v. Samsung Electronics Co., Ltd*., No. 8:20-cv-993-MCS (C.D. Cal.) action. The referenced documents speak for themselves and therefore no response is necessary. Except as expressly admitted, Netlist denies the allegations of this paragraph.

36. Paragraph 36 purports to quote and reference a webpage containing Netlist's press release. The content on that cited webpage speaks for itself and therefore no response is necessary. Except as expressly admitted, Netlist denies the allegations of this paragraph.

37. With respect to the first two sentences of paragraph 37, Netlist is without knowledge sufficient to admit or deny the allegations in Paragraph 37 and, therefore, denies. The third sentence of paragraph 37 states a legal conclusion and therefore no response is necessary; but to the extent that further response is necessary, Netlist denies.

38. Denied.

39. The first sentence of paragraph 39 purports to reference Netlist's pleadings filed in one or more past actions involving SK hynix. The pleadings of the referenced actions speak for themselves, and therefore no response is needed. The remaining allegations in paragraph 39 purport to reference certain *Inter Partes* Review ("IPR") proceedings. The referenced petitions

and proceedings speak for themselves, and therefore no response is needed. Except as expressly admitted, Netlist denies the allegations of this paragraph.

40. Based on the Court's Order dismissing Plaintiffs' claims relating to the '912 patent, D.I. 38, no response is needed to this paragraph.

41. Based on the Court's Order dismissing Plaintiffs' claims relating to the '912 patent, D.I. 38, no response is needed to this paragraph.

42. Based on the Court's Order dismissing Plaintiffs' claims relating to the '912 patent, D.I. 38, no response is needed to this paragraph.

43. Based on the Court's Order dismissing Plaintiffs' claims relating to the '912 patent, D.I. 38, no response is needed to this paragraph.

44. Based on the Court's Order dismissing Plaintiffs' claims relating to the '912 patent, D.I. 38, no response is needed to this paragraph.

45. Based on the Court's Order dismissing Plaintiffs' claims relating to the '912 patent, D.I. 38, no response is needed to this paragraph.

46. Based on the Court's Order dismissing Plaintiffs' claims relating to the '339, '506 and '918 patents, D.I. 38, no response is needed to this paragraph. To the extent a response is necessary, with respect to the first sentence of paragraph 46, Netlist admits that it filed a lawsuit against SEC, SSI, and Samsung Electronics America, Inc. ("SEA") on December 20, 2021 under the caption *Netlist, Inc. v. Samsung Electronics Co.*, Ltd., No. 2:21-cv-00463 (E.D. Tex.) (the "Texas Infringement Action"). The remaining allegations in paragraph 46 purport to reference Netlist's pleadings in the Texas Infringement Action. These pleadings speak for themselves, and therefore no response is needed. Except as expressly admitted, Netlist denies the allegations of this paragraph.

47. Based on the Court's Order dismissing Plaintiffs' claims relating to the '339, '506 and '918 patents, D.I. 38, no response is needed to this paragraph. To the extent a response is necessary, paragraph 47 purports to quote a pleading in the Texas Infringement Action. That pleading speaks for itself, and therefore no response is needed.

48. Based on the Court's Order dismissing Plaintiffs' claims relating to the '339, 506 and '918 patents, D.I. 38, no response is needed to this paragraph. To the extent a response is necessary, paragraph 48 purports to reference Netlist's complaint in the Texas Infringement Action. The complaint speaks for itself, and therefore no response is needed. With the respect to the last sentence, Netlist does not have sufficient knowledge to admit or deny what Samsung expected, and therefore, denies.

49. Based on the Court's Order dismissing Plaintiffs' claims relating to the '339, '506 and '918 patents, D.I. 38, no response is needed to this paragraph. To the extent a response is necessary, paragraph 49 purports to reference Netlist's complaint in the Texas Infringement Action and its motion to dismiss filed in this instant Action. These documents speak for themselves, and therefore no response is needed. To the extent further response is necessary, Netlist denies.

50. Based on the Court's Order dismissing Plaintiffs' claims relating to the '339, '506 and '918 patents, D.I. 38, no response is needed to this paragraph. To the extent a response is necessary, Netlist denies the allegation in this paragraph.

51. Based on the Court's Order dismissing Plaintiffs' claims relating to the '339, '506 and '918 patents, D.I. 38, no response is needed to this paragraph. To the extent a response is necessary, Netlist denies the allegation in this paragraph.

52. Paragraph 52 purports to reference separate lawsuits or IPR proceedings. The pleadings and other filings in the separate lawsuits or IPR proceedings speak for themselves. With

respect to Plaintiffs' allegation that Micron is a "competitor of Samsung," Netlist is without knowledge sufficient to admit or deny and therefore denies. With respect to the remaining allegations in paragraph 52, Netlist denies.

53. The allegations in this paragraph state a legal conclusion to which no response is required.

54. With respect to the first sentence of paragraph 54, Netlist denies. The remaining allegations in paragraph 54 purport to quote or reference a letter dated October 15, 2020 or documents created, circulated, and/or filed in separate actions. These referenced letter and documents speak for themselves, and therefore no response is needed. To the extent further response is necessary, Netlist denies.

55. Based on the Court's Order dismissing Plaintiffs' claims relating to the '912 patent, D.I. 38, no response is needed to this paragraph. To the extent a response is necessary, paragraph 55 purports to reference Netlist's pleadings in the Google Action. These documents speak for themselves, and therefore no response is needed. Except as expressly admitted, Netlist denies the allegations of this paragraph.

56. Based on the Court's Order dismissing Plaintiffs' claims relating to the '506 and '339 patents, D.I. 38, no response is needed to this paragraph. To the extent a response is necessary, paragraph 56 purports to quote a pleading in the Texas Infringement Action. The pleading speaks for itself, and therefore no response is needed. Except as expressly admitted, Netlist denies the allegations of this paragraph.

57. Based on the Court's Order dismissing Plaintiffs' claims relating to the '918 patent and '019 application, D.I. 38, no response is needed to this paragraph. To the extent a response is necessary, paragraph 57 purports to quote and reference a pleading in the Texas Infringement

Action. The pleading speaks for itself, and therefore no response is needed. Except as expressly admitted, Netlist denies the allegations of this paragraph.

58. Based on the Court's Order dismissing Plaintiffs' claims relating to the '918 patent and '019 application, D.I. 38, no response is needed to this paragraph. To the extent a response is necessary, Netlist admits that Plaintiffs filed this instant action seeking certain declaratory judgment reliefs. Netlist denies that Plaintiffs are entitled to the relief they seek. The remaining allegations of paragraph 58 state legal conclusions to which no response is required. To the extent any response is necessary, Netlist denies.

59. Denied.

60. With respect to the first sentence of paragraph 60, Netlist admits that the '523 patent relates to memory subsystems and, more specifically, a self-testing architecture for memory modules that utilizes certain on-board components to conduct testing functions without substantial system memory controller involvement. The remaining allegations of paragraph 60 purport to reference the '523 patent, which speaks for itself. Except as expressly admitted, Netlist denies the allegations of this paragraph.

61. Paragraph 61 purports to reference the '523 patent, which speaks for itself. Except as expressly admitted, Netlist denies the allegations of this paragraph.

62. Paragraph 62 purports to reference the '523 patent, which speaks for itself. Except as expressly admitted, Netlist denies the allegations of this paragraph.

63. The first sentence of paragraph 63 contains legal argument to which no response is required. The remaining allegations of paragraph 63 purport to quote JESD82-32, which speaks for itself. Except as expressly admitted, Netlist denies the allegations of this paragraph.

64. Denied.

65. Paragraph 65 purports to reference the '595 patent, which speaks for itself. Except as expressly admitted, Netlist denies the allegations of this paragraph.

66. Paragraph 66 purports to reference the '595 patent, which speaks for itself. Except as expressly admitted, Netlist denies the allegations of this paragraph.

67. Paragraph 67 purports to reference the '595 patent, which speaks for itself. Except as expressly admitted, Netlist denies the allegations of this paragraph.

68. Paragraph 68 purports to reference the '595 patent, which speaks for itself. Except as expressly admitted, Netlist denies the allegations of this paragraph.

69. Paragraph 69 purports to reference the '595 patent, which speaks for itself. Except as expressly admitted, Netlist denies the allegations of this paragraph.

70. The first sentence of paragraph 70 contains legal argument to which no response is required. The remaining allegations of paragraph 63 purports to quote JESD82-31, which speaks for itself. Except as expressly admitted, Netlist denies the allegations of this paragraph.

71. Denied.

72–76. Based on the Court's Order dismissing Plaintiffs' claims relating to the '912 patent, D.I. 38, no response is needed to paragraphs 72–76. To the extent further response is necessary, Netlist denies.

77–81. Based on the Court's Order dismissing Plaintiffs' claims relating to the '506 patent, D.I. 38, no response is needed to paragraphs 77–81. To the extent further response is necessary, Netlist denies.

82–88. Based on the Court's Order dismissing Plaintiffs' claims relating to the '339 patent, D.I. 38, no response is needed to paragraphs 82–88. To the extent further response is necessary, Netlist denies.

89–93. Based on the Court's Order dismissing Plaintiffs' claims relating to the '918 patent, D.I. 38, no response is needed to paragraphs 89–93. To the extent further response is necessary, Netlist denies.

94. The allegations of Paragraph 94 state a legal conclusion to which no response is required. To the extent further response is necessary, Netlist denies.

95. Denied.

96. Denied.

97. Denied.

98. Netlist admits that it is a member of JEDEC. Netlist is without knowledge sufficient to admit or deny the remaining allegations in Paragraph 98 and, therefore, denies.

99. Netlist is without knowledge sufficient to admit or deny the allegations in Paragraph 99 and, therefore, denies.

100. Netlist is without knowledge sufficient to admit or deny the allegations in Paragraph 100 and, therefore, denies.

101. Netlist admits that JEDEC members participate in the standard-setting process through certain committees and subcommittees, including by contributing to and/or voting on technical proposals to be incorporated into the JEDEC standards. With respect to the remaining allegations in paragraph 101, Netlist is without knowledge sufficient to admit or deny and therefore denies.

102. Netlist is without knowledge sufficient to admit or deny the allegations in the first sentence of paragraph 102 and, therefore, denies. The remaining allegations of paragraph 102 state legal conclusions to which no response is required. To the extent any response is necessary, Netlist denies.

103. Paragraph 103 contains argument or legal conclusion to which no response is required. To the extent any response is necessary, Netlist denies.

104. Paragraph 104 contains argument or legal conclusion to which no response is required. To the extent any response is necessary, Netlist denies.

105. Paragraph 105 contains argument or legal conclusion to which no response is required. To the extent any response is necessary, Netlist denies.

106. Paragraph 106 contains argument or legal conclusion to which no response is required. To the extent any response is necessary, Netlist denies.

107. Paragraph 107 contains argument or legal conclusion to which no response is required. To the extent any response is necessary, Netlist denies.

108. Paragraph 108 contains argument or legal conclusion to which no response is required. To the extent any response is necessary, Netlist denies.

109. Paragraph 109 contains argument or legal conclusion to which no response is required. To the extent any response is necessary, Netlist denies.

110. Paragraph 110 contains argument or legal conclusion to which no response is required. To the extent any response is necessary, Netlist denies.

111. Paragraph 111 contains argument or legal conclusion to which no response is required. To the extent any response is necessary, Netlist denies.

112. Paragraph 112 contains argument or legal conclusion to which no response is required. To the extent any response is necessary, Netlist denies.

113. Paragraph 113 contains argument or legal conclusion to which no response is required. To the extent any response is necessary, Netlist denies.

114. Paragraph 114 contains argument or legal conclusion to which no response is required. To the extent any response is necessary, Netlist denies.

115. Paragraph 115 contains argument or legal conclusion to which no response is required. To the extent any response is necessary, Netlist denies.

116. Paragraph 116 contains argument or legal conclusion to which no response is required. To the extent any response is necessary, Netlist denies.

117. Admitted.

118. Netlist admits that it is a member of JEDEC. Paragraph 118 purports to reference documents and/or communications regarding Netlist's membership in certain JEDEC committees. The documents and/or communications speak for themselves. Except as expressly admitted, Netlist denies the allegations of paragraph 118.

119. Netlist admits that it is a member of JEDEC. Netlist is without knowledge sufficient to admit or deny the remaining allegations in paragraph 119 and, therefore, denies.

120. Netlist admits that it has communicated with JEDEC regarding Netlist's patents. Except as otherwise expressly admitted, Netlist denies the remaining allegations of paragraph 120.

121. Paragraph 121 contains argument or legal conclusion to which no response is required. With respect to Plaintiffs' reference a document relating to the '434 patent Netlist submitted to JEDEC dated April 7, 2016, and a purported JEDEC policy, the document and policy speak for themselves, and therefore, no response is necessary. Except as expressly admitted, Netlist denies the allegations of paragraph 121.

122. Paragraph 122 contains argument or legal conclusion to which no response is required. With respect to Plaintiffs' reference a document relating to the '837 patent Netlist purportedly submitted to the JEDEC dated April 7, 2016, and a purported JEDEC policy, the

document and policy speak for themselves, and therefore, no response is necessary. Except as expressly admitted, Netlist denies the allegations of paragraph 122.

123. Because this Court has dismissed Plaintiffs' claims relating to the '912 patent, no response is needed for paragraph 123. To the extent any response is necessary, Netlist denies.

124. Because this Court has dismissed Plaintiffs' claims relating to the '912 patent, no response is needed for paragraph 124. To the extent any response is necessary, Netlist denies.

125. Because this Court has dismissed Plaintiffs' claims relating to the '912 patent, no response is needed for paragraph 125. To the extent any response is necessary, Netlist denies.

126. Because this Court has dismissed Plaintiffs' claims relating to the '912 patent, no response is needed for paragraph 126. To the extent any response is necessary, Netlist denies.

127. Because this Court has dismissed Plaintiffs' claims relating to the '506 patent, no response is needed for paragraph 127. To the extent any response is necessary, Netlist denies.

128. Because this Court has dismissed Plaintiffs' claims relating to the '339 patent, no response is needed for paragraph 128. To the extent any response is necessary, Netlist denies.

129. Because this Court has dismissed Plaintiffs' claims relating to the '339 patent, no response is needed for paragraph 129. To the extent any response is necessary, Netlist denies.

130. Because this Court has dismissed Plaintiffs' claims relating to the '918 patent, no response is needed for paragraph 130. To the extent any response is necessary, Netlist denies.

131. Because this Court has dismissed Plaintiffs' claims relating to the '918 patent, no response is needed for paragraph 131. To the extent any response is necessary, Netlist denies.

132. Because this Court has dismissed Plaintiffs' claims relating to the '918 patent, no response is needed for paragraph 132. To the extent any response is necessary, Netlist denies.

133. Because this Court has dismissed Plaintiffs' claims relating to the '019 application, no response is needed for paragraph 133. To the extent any response is necessary, Netlist denies.

134. Because this Court has dismissed Plaintiffs' claims relating to the '019 application, no response is needed for paragraph 134. To the extent any response is necessary, Netlist denies.

135. Because this Court has dismissed Plaintiffs' claims relating to the '019 application, no response is needed for paragraph 135. To the extent any response is necessary, Netlist denies.

136. Paragraph 136 contains argument or legal conclusion to which no response is required. To the extent any response is necessary, Netlist denies. Netlist denies that Samsung can enforce the RAND obligations against Netlist given Samsung's material and extensive hold-out behavior.

137. Denied.

138. Paragraph 138 contains argument or legal conclusion to which no response is required. To the extent paragraph 138 references to or quotes Netlist's pleadings or other filings in other separate litigations, the referenced documents speak for themselves and therefore, no response is necessary. To the extent any response is necessary, Netlist denies.

139. Denied.

140. Denied.

COUNT I

141. Netlist incorporates by reference its responses in the preceding paragraphs as if fully set forth herein.

142. Netlist admits that Plaintiffs purport to have attached a true and correct copy of the '523 patent certification as Exhibit 1 to the FAC. The '523 patent speaks for itself. Netlist further admits that Netlist owns by assignment all rights, title, and interest in and to the '523 patent. Netlist

further admits that the USPTO issued the '523 patent on February 26, 2019, and that the title of the '523 patent is "Multi-Mode Memory Module with Data Handlers."

143. Paragraph 143 purports to reference the content of the '523 patent and tabulate the language of claim 1 of the '523 patent. The '523 patent speaks for itself, and therefore a response is unnecessary. Except as expressly admitted, Netlist denies the allegations of paragraph 143.

144. Netlist admits that by filing its Counterclaims, Netlist first alleges that Samsung has infringed and continues to infringe one or more claims of the '523 patent. To the extent further response is necessary, Netlist denies.

145. Denied.

146. Paragraph 146 purports to reference the content of the '523 patent. The '523 patent speaks for itself, and therefore a response is unnecessary. The allegations in this paragraph state legal conclusions to which no response is required. Except as expressly admitted, Netlist denies the allegations of paragraph 146.

147. Paragraph 147 purports to reference the content of the '523 patent. The '523 patent speaks for itself, and therefore a response is unnecessary. The allegations in this paragraph also state legal conclusions to which no response is required. Except as expressly admitted, Netlist denies the allegations of paragraph 147.

148. Denied.

149. Denied.

150. Denied.

151. Netlist denies that Plaintiffs are entitled to any relief.

COUNT II

152. Netlist incorporates by reference its responses in the preceding paragraphs as if fully set forth herein.

153. Netlist admits that Plaintiffs purport to have attached the '595 patent certification as Exhibit 2 to the FAC. The '595 patent speaks for itself. Netlist further admits that Netlist owns by assignment all rights, title, and interest in and to the '595 patent. Netlist further admits that the patent Office issued the '595 patent on November 12, 2019 and that the title of the '595 patent is "Memory Module Having An Open-Drain Output Pin For Parity Error In A First Mode And For Training Sequences In A Second Mode."

154. Paragraph 154 purports to reference the content of the '595 patent and tabulate the language of claim 1 of the '595 patent. The '595 patent speaks for itself, and therefore a response is unnecessary. Except as expressly admitted, Netlist denies the allegations of paragraph 154.

155. Netlist admits that by filing its Counterclaims, Netlist alleges that Samsung has infringed and continues to infringe one or more claims of the '595 patent. To the extent further response is necessary, Netlist denies.

156. Denied.

157. Paragraph 157 purports to reference the content of the '595 patent. The '595 patent speaks for itself, and therefore a response is unnecessary. The allegations in this paragraph state legal conclusions to which no response is required. Except as expressly admitted, Netlist denies the allegations of paragraph 157.

158. Paragraph 158 purports to reference the content of the '595 patent. The '595 patent speaks for itself, and therefore a response is unnecessary. The allegations in this paragraph state

legal conclusions to which no response is required. Except as expressly admitted, Netlist denies the allegations of paragraph 158.

159. Denied.

160. Denied.

161. Denied.

162. Netlist denies that Plaintiffs are entitled to any relief.

COUNT III

163. Netlist incorporates by reference its responses in the preceding paragraphs as if fully set forth herein.

164. Netlist admits that Plaintiffs purport to have attached the '218 patent certification as Exhibit 3 to the FAC. The '218 patent speaks for itself, and therefore a response is unnecessary. Netlist further admits that Netlist owns by assignment all rights, title, and interest in and to the '218 patent. Netlist further admits that the USPTO issued the '218 patent on January 2, 2018 and that the title of the '218 patent is "Memory Module And Methods For Handshaking With A Memory Controller."

165. Paragraph 165 purports to reference the content of the '218 patent and tabulate the language of claim 1 of the '218 patent. The '218 patent speaks for itself, and therefore a response is unnecessary. Except as expressly admitted, Netlist denies the allegations of paragraph 165.

166. Netlist admits that by filing its Counterclaims, Netlist alleges that Samsung has infringed and continues to infringe one or more claims of the '218 patent. Except as expressly admitted, Netlist denies the allegations of paragraph 165.

167. Denied.

168. Paragraph 168 purports to reference the content of the '218 patent. The '218 patent speaks for itself, and therefore a response is unnecessary. The allegations in this paragraph state legal conclusions to which no response is required. Except as expressly admitted, Netlist denies the allegations of paragraph 168.

169. Paragraph 169 purports to reference the content of the '218 patent. The '218 patent speaks for itself, and therefore a response is unnecessary. The allegations in this paragraph state legal conclusions to which no response is required. Except as expressly admitted, Netlist denies the allegations of paragraph 169.

170. Paragraph 170 purports to reference the content of the '218 patent. The '218 patent speaks for itself, and therefore a response is unnecessary. The allegations in this paragraph state legal conclusions to which no response is required. Except as expressly admitted, Netlist denies the allegations of paragraph 170.

171. Denied.

172. Denied.

173. Denied.

174. Netlist denies that Plaintiffs are entitled to any relief.

COUNT IV

Based on the Court's Order dismissing Count IV, D.I. 38, no response is needed to paragraphs 175–189. To the extent any response is necessary, Netlist denies.

COUNT V

Based on the Court's Order dismissing Count V, D.I. 38, no response is needed to paragraphs 190–199. To the extent any response is necessary, Netlist denies.

COUNT VI

Based on the Court's Order dismissing Count VI, D.I. 38, no response is needed to paragraphs 200–209. To the extent any response is necessary, Netlist denies.

COUNT VII

Based on the Court's Order dismissing Count VII, D.I. 38, no response is needed to paragraphs 210–220. To the extent any response is necessary, Netlist denies.

COUNT VIII

221. Netlist incorporates by reference its responses in the preceding paragraphs as if fully set forth herein.

222. Denied.

223. Netlist admits that Hyun Lee, Jayesh Bhakta and Soonju Choi are the named inventors of the '523 patent and they submitted oaths or declarations. The '523 patent and the cited documents speak for themselves, and therefore no response is needed. Except as expressly admitted, Netlist denies the remaining allegations of paragraph 223.

224. Noel Whitley was, during the prosecution of the application that issued as the '523 patent, an employee and/or contractor for Netlist. Except as expressly admitted, Netlist denies the remaining allegations of this paragraph.

225. Marwan Fawal was, during the prosecution of the application that issued as the '523 patent, a contractor for Netlist. Except as expressly admitted, Netlist denies the remaining allegations of this paragraph.

226. Gail Sasaki was, during the prosecution of the application that issued as the '523 patent, an employee and/or contractor for Netlist. To the extent that paragraph 226 references a power of attorney submitted by Netlist to the USPTO, that power of attorney document speaks for

itself, and therefore a response is unnecessary. Except as expressly admitted, Netlist denies the remaining allegations of this paragraph.

227. Netlist admits that Jamie Zheng was involved in the prosecution of the '523 patent and otherwise denies.

228. Denied.

229. The allegations in this paragraph state a legal conclusion to which no response is required. To the extent any response is necessary, Netlist denies.

230. Paragraph 230 purports to reference the '523, '434, '501, and '064 patents, which speak for themselves and therefore no response is required.

231. Paragraph 231 purports to reference the '523 patent, the '912 patent, and their applications, which speak for themselves and therefore no response is required. Netlist admits that Jayesh Bhakta is a named inventor on the '912 patent. Netlist admits that U.S. Patent Application No. 2006/0277355 to Ellsberry et al. appears in the '912 patent's "References Cited" list and was one of the references mentioned by the examiner in the Notice of Allowability. Except as expressly admitted, Netlist denies the remaining allegations of this paragraph.

232. Denied.

233. Netlist is without knowledge sufficient to admit or deny the allegations in this paragraph of the Complaint and, therefore, denies.

234. Netlist is without knowledge sufficient to admit or deny the allegations in this paragraph of the Complaint and, therefore, denies.

235. Denied.

236. Netlist is without knowledge sufficient to admit or deny the allegations in this paragraph of the Complaint and, therefore, denies.

237. Admitted.

238. Paragraph 238 purports to reference Netlist's filings in connection with the application No. 14/229,844. The application record speaks for itself. Netlist admits that it complied with its duty of disclosure and submitted information disclosure statements on at least August 7, 2014, August 10, 2014, December 24, 2014, February 16, 2016, February 17, 2016, February 18, 2016, July 13, 2016, March 24, 2017, September 5, 2017, May 17, 2018, August 28, 2018, October 16, 2018, and January 30, 2019.

239. Paragraph 239 purports to reference statements made in an Office Action dated March 9, 2016. The application record speaks for itself and therefore no response is required. In particular, Netlist references pages 11-15 of the applicants' July 11, 2016 responses to the March 9, 2016 Office Action which explained the relevance of the disclosed references in earlier information disclosure statements. To the extent any further response is necessary, Netlist denies.

240. Denied.

241. Denied. Netlist identifies, for example, the applicants' July 11, 2016 responses to the March 9, 2016 Office Action.

242. Paragraph 242 purports to quote statements of the examiner in connection with the prosecution of the '523 patent. The referenced document speaks for itself and therefore no response is required. To the extent any response is necessary, Netlist denies.

243. Netlist admits that on August 31 and September 1, 2016, Netlist filed complaints against SK hynix in the Central District of California and the U.S. International Trade Commission asserting U.S. Pat. Nos. 8,689,064; 8,001,434; and 8,359,501 against SK hynix.

244. Netlist admits that SK Hynix filed IPR2017-00560, IPR2017-00561 and IPR2017-00562 against U.S. Pat. Nos. 8,689,064; 8,001,434; and 8,359,501 on January 3, 2017, January 5,

2017, and January 3, 2017, respectively. Except as expressly admitted, Netlist denies the remaining allegations of this paragraph.

245. Paragraph 245 purports to reference filings in connection with the prosecution of the '523 patent, and the filings speak for themselves and therefore no response is required. Netlist admits that on March 21, 2017, in response to the Office Action dated October 20, 2016, it requested continued examination and submitted a list of amended claims. Except as expressly admitted, Netlist denies the remaining allegations of this paragraph.

246. Netlist admits that it submitted an information disclosure statement on March 24, 2017 to comply with its disclosure duty. The information disclosure statement speaks for itself and therefore no response is required. Except as expressly admitted, Netlist denies the remaining allegations of this paragraph.

247. Netlist admits that on April 4, 2017, the Office issued a non-final Office Action allowing then pending claims 1-8, 10-12, 26-29 and 36 and rejecting pending claims 37-48. The examiner also signed form 1449, acknowledging that the Office has considered the references disclosed on the information disclosure statement. Except as expressly admitted, Netlist denies the remaining allegations of this paragraph.

248. Netlist admits that on September 5, 2017, it amended the allowed claims 1-5, 7, 10-12, 26-28 and 36 for clarity; cancelled pending claims 6, 29, and 37-48; and added new claims 49-75. Except as expressly admitted, Netlist denies the remaining allegations of this paragraph.

249. Netlist admits that on September 5, 2017, in compliance with its duty of disclosure, it submitted an information disclosure statement. The information disclosure statement speaks for itself and therefore no response is required. Except as expressly admitted, Netlist denies the remaining allegations of this paragraph.

250. Netlist admits that on December 8, 2017, the examiner issued an Office Action imposing a restriction/election requirement and rejected then pending claims under 35 U.S.C. §§ 101 and/or 112. On the same date, the examiner signed form 1449 to acknowledge the Office's consideration of the applicants' disclosed references. Except as expressly admitted, Netlist denies the remaining allegations of this paragraph.

251. Paragraph 251 purports to reference events and/or filings in a separate ITC proceeding and because of the confidentiality of the proceeding and the protective order in place, Netlist and the undersigned are without knowledge sufficient to admit or deny the contents of the confidential filings, and on that basis, deny. To the extent paragraph 251 references the public version of the filings, those filings speak for themselves and therefore no response is required. Except as expressly admitted, Netlist denies the remaining allegations of this paragraph.

252. Denied.

253. Paragraph 253 purports to reference filings in a separate ITC proceeding that contains confidential information. To the extent paragraph 253 references the public version of the confidential filings, those filings speak for themselves and therefore no response is required. Except as expressly admitted, Netlist denies the remaining allegations of this paragraph.

254. The first and third sentences of paragraph 254 purports to reference an IPR petition filed by a third party. The petition speaks for itself, and therefore no response is required. To the extent any response is necessary, Netlist denies. The second sentence of paragraph 254 reference the U.S. Patent No. 9,606,907 (the "'907 patent") and its named inventors, and the patent certificate speaks for itself. Netlist admits, however, the '907 patent lists Hyun Lee and Jayesh Bhakta as inventors. Except as expressly admitted, Netlist denies the remaining allegations of this paragraph.

255. Netlist admits that on February 8, 2018, it filed "Certification and Request for Consideration Under the After Final Consideration Pilot Program 2.0." Its request included amended claims and remarks in response to the December 8, 2017 Office Action. Except as expressly admitted, Netlist denies the remaining allegations of this paragraph.

256. On February 15, 2018, in response to the Office's Advisory Action dated February 14, 2018, Netlist filed a request for continued examination, attaching amended claims and responses that were largely the same as those submitted on February 8, 2018. Except as expressly admitted, Netlist denies the remaining allegations of this paragraph.

257. Paragraph 257 purports to reference an *Ex parte Quayle* action in connection with the prosecution of the '523 patent. The examiner's action speaks for itself. In the Office Action Summary, the Office allowed pending claims 1-12, 28, 36, 58-63, 66, 76-83, and 85-88, and objected to claims 64, 65 and 84. The Office Action also included examiner's amendment to claim 58. Except as expressly admitted, Netlist denies the remaining allegations of this paragraph.

258. On May 2, 2018, Netlist amended pending claims 63, 64, 66, 76, 79, 84 and 88 for clarity and/or correction of typographical errors. Netlist did not amend the remaining pending claims. Except as expressly admitted, Netlist denies the remaining allegations of this paragraph.

259. Netlist admits that on May 17, 2018, it submitted an Information Disclosure Statement ("IDS"). The IDS speaks for itself and therefore no response is required. To the extent any response is necessary, Netlist denies.

260. Netlist admits that on August 28, 2018, it submitted an IDS. The IDS speaks itself and therefore no response is required. To the extent any response is necessary, Netlist denies.

261. Admitted.

262. Paragraph 262 purports to reference filings in connection with the prosecution of the '523 patent. The interview summary speaks for itself and therefore no response is required. Except as expressly admitted, Netlist denies the remaining allegations of this paragraph.

263. Admitted.

264. Paragraph 264 purports to reference certain separate proceedings relating to the '907 patent without providing the source. These proceedings and/or filings, if existing, speak for themselves. Netlist further notes that to the extent that the '907 patent family's validity is even relevant to the '523 patent, the Office issued the '339 patent—a continuation of the '907 patent—over Ellsberry. Except as expressly admitted, Netlist denies the remaining allegations of this paragraph.

265. Denied.

266. Netlist admits that on August 21, 2020, SK Hynix filed IPR2020-01421 against the '523 patent. Netlist also admits that among the references submitted with IPR2020-01421 is U.S. Pat. No. 7,310,752 to Jeddeloh. As to the remainder of the paragraph, the filings in IPR2020-01421 speak for themselves and therefore no response is required.

267. Paragraph 267 purports to reference filings in connection with an IPR petition against the '523 patent filed by a third party. The filings speak for themselves, and no response is required. To the extent any response is necessary, Netlist denies.

268. Netlist admits that on March 16, 2021, the PTAB instituted the inter partes review of the '523 patent. The proceeding is subsequently terminated. Except as expressly admitted, Netlist denies the remaining allegations of this paragraph.

269. Denied.

270. Denied.

271. Denied.

272. Denied.

273. Denied.

274. Denied.

275. Denied.

276. Denied.

277. Denied.

278. Denied.

COUNT IX

279. Netlist incorporates by reference its responses in the preceding paragraphs as if fully set forth herein.

280. Denied.

281. Netlist admits that Hyun Lee is the sole named inventor of the '218 and '595 patents, and he submitted oaths or declarations in support of the applications. The oaths or declarations speak for themselves, and no response is required.

282. Noel Whitley was, during the prosecution of the applications that issued as the '218 and '595 patents, an employee and/or contractor for Netlist. Except as expressly admitted, Netlist denies the allegations of this paragraph.

283. Marwan Fawal was, during the prosecution of the applications that issued as the '218 and '595 patents, a contractor for Netlist. Except as expressly admitted, Netlist denies the allegations of this paragraph.

284. Gail Sasaki was, during the prosecution of the applications that issued as the '218 and '595 patents, an employee and/or contractor for Netlist. To the extent that paragraph 284

references a power of attorney submitted by Netlist to the USPTO, that power of attorney document speaks for itself, and therefore a response is unnecessary. Except as expressly admitted, Netlist denies the allegations of this paragraph.

285. Netlist admits that Jamie Zheng was involved in the prosecution of the '218 and '595 patents, and otherwise denies.

286. Denied.

287. The allegations in this paragraph state a legal conclusion to which no response is required. To the extent any response is necessary, Netlist denies.

288. Paragraph 288 purports to reference information stated in the certificates of the '218 and '595 patents, which speak for themselves. No response is therefore required. To the extent any response is necessary, Netlist denies.

289. Netlist admits that, on August 10, 2016, it filed a terminal disclaimer for Application No. 15/088,115 (which issued as the '218 patent) over U.S. Pat. Nos. 8,489,837 and 9,311,116. The claims were then amended several times before issuing on January 2, 2018. Netlist also admits that, on November 28, 2018, it filed a terminal disclaimer for then pending claims of Application No. 15/857,553 (issued as the '595 patent) over U.S. Pat. Nos. 8,489,837; 9,311,116; and the '218 patent. Netlist admits that, on August 3, 2016, a terminal disclaimer was filed for Application No. 15/169,745 (which issued as U.S. Pat. No. 9,535,623) over claims pending in Application No. 15/088,115 and U.S. Pat. No. 9,311,116. As noted above, the claims of the '115 application underwent several amendments before emerging as the issued claims of the '218 patent. Except as expressly admitted, Netlist denies the remaining allegations of this paragraph.

290. Netlist is without knowledge sufficient to admit or deny the allegations in paragraph 290 and therefore, denies.

291. Denied.

292. Netlist admits that Plaintiffs contend that they have attached a true and correct copy of JESD82-29 as Exhibit 30 to the FAC. The document attached as Exhibit 30 to the FAC speaks for itself. Netlist is without knowledge sufficient to admit or deny the remaining allegations in paragraph 292 and therefore, denies.

293. Netlist admits that Plaintiffs contend that they have attached a true and correct copy of a draft of JESD82-29 as Exhibit 31 to the FAC. The document attached as Exhibit 31 to the FAC speaks for itself. Netlist is without knowledge sufficient to admit or deny the remaining allegations in paragraph 293 and therefore, denies.

294. Denied.

295. Netlist admits that Plaintiffs contend that they have attached a true and correct copy of a Committee Letter Ballot as Exhibit 32 to the FAC. The document attached as Exhibit 32 to the FAC speaks for itself. To the extent any response is necessary, Netlist denies.

296. Netlist admits that Plaintiffs contend that they have attached a true and correct copy of a Committee Letter Ballot as Exhibit 33 to the FAC. The document attached as Exhibit 33 to the FAC speaks for itself. To the extent any response is necessary, Netlist denies.

297. Denied.

298. Denied.

299. Paragraph 299 purports to reference a provisional application to which the '218 and '595 patents claim priority. The referenced provisional application speaks for itself. Netlist further admits that the U.S Application No. 61/186,799 was filed on June 12, 2009.

300. Paragraph 300 purports to quote Netlist's filing in a separate litigation and the filing speaks for itself. To the extent any response is necessary, Netlist denies.

301. Paragraph 301 purports to reference Netlist's filings in a separate litigation and the filing speaks for itself. The referenced action did not involve the '218 or the '595 patent. To the extent that Samsung's arguments and legal conclusions require a response, Netlist denies.

302. Paragraph 302 purports to reference a provisional application to which the '218 and '595 patents claim priority. The referenced provisional application speaks for itself. No response is required.

303. Paragraph 303 purports to reference Netlist's statement without providing a source. As a result, Netlist cannot verify the information provided and, therefore, denies.

304. Netlist is without knowledge sufficient to admit or deny the allegations in paragraph 304 and therefore, denies.

305. Netlist admits that that Plaintiffs contend that they have attached a true and correct copy of a document titled "MB Initialization sequence Item 142.35" is attached as Exhibit 34 to Plaintiffs' FAC and otherwise denies.

306. The allegations in this paragraph state a legal conclusion to which no response is required. To the extent any response is necessary, Netlist denies.

307. Netlist is without knowledge sufficient to admit or deny the allegations in paragraph 307 and therefore, denies.

308. Netlist is without knowledge sufficient to admit or deny the allegations in paragraph 308 and therefore, denies.

309. Netlist admits that a purported copy of a document titled "Memory Buffer Membist for LRDIMM DDR MB TG item # 142.43" is attached as Exhibit 35 to Plaintiffs' FAC and otherwise denies.

310. The allegations in this paragraph state a legal conclusion to which no response is required. To the extent any response is necessary, Netlist denies.

311. Denied.

312. Admitted.

313. Admitted.

314. Admitted.

315. Admitted.

316. Admitted.

317. Netlist admits that SK hynix filed IPR2018-00303 against U.S. Pat. No. 9,535,623 on December 14, 2017. Netlist also admits that included in SK hynix's exhibit list are U.S. Patent Application Publication No. 2008/0098277 ("Hazelzet"), U.S. Patent No. 8,139,430 ("Buchmann"), U.S. Patent Application Publication No. 2008/0155378 ("Talbot"), and U.S. Patent Application Publication No. 2008/0155378 ("Amidi"). With respect to the remainder of the paragraph, SK hynix's filings speak for themselves and no response is required. To the extent further response is required, Netlist denies.

318. Netlist admits that the '218 patent was issued on January 2, 2018, but otherwise denies.

319. Netlist admits that it filed Application No. 15/857,553 on December 28, 2017, which issued as the '595 patent. It otherwise denies the allegation in the paragraph.

320. Netlist agrees that between March 1 and March 21, 2019, it disclosed materials related to IPR2020-00303, including the petition, the final written decision, and references to the Office during the prosecution of the '595 patent. The Office issued multiple notices of allowances after that. Netlist otherwise denies the allegation in the paragraph.

321. Admitted.

322. Netlist admits that on March 1, 2019 that it filed with the USPTO an Amendment and Request for Continued Examination in connection with the prosecution of the '595 patent, and Netlist's filing speaks for itself. To the extent further response is required, Netlist denies.

323. Admitted.

324. Netlist admits that, on July 1, 2019, it filed with the USPTO a Request for Continued Examination in connection with the prosecution of the '595 patent, and Netlist's filing speaks for itself. To the extent further response is required, Netlist denies.

325. Admitted.

326. Admitted.

327. Paragraph 327 purports to reference filings and briefings in an ITC action and these documents speak for themselves. To the extent further response is required, Netlist denies.

328. Netlist incorporates by reference its response to paragraph 317.

329. Paragraph 329 purports to reference decisions or filings in connection with an IPR petition filed by a third party against a patent unasserted in this Action, and the referenced documents speak for themselves. To the extent further response is required, Netlist denies.

330. Paragraph 330 purports to reference a PTAB decision in connection with an IPR petition filed by a third party against a patent unasserted in this Action and the referenced documents speak for themselves. To the extent further response is required, Netlist denies.

331. Denied.

332. Netlist admits that SK hynix filed IPR2020-01042 and IPR2020-01044 against the '218 and '595 patents respectively on June 9, 2020. Netlist also admits that the exhibits

accompanying SK hynix's petitions included the mentioned references. Except as expressly admitted, Netlist denies the allegations in this paragraph.

333. Paragraph 333 purports to reference IPR petitions filed by a third party against the '218 and '595 patents and the petitions speak for themselves. To the extent further response is required, Netlist denies.

334. Netlist admits that the PTAB instituted trials in IPR2020-01042 and IPR2020-01044 after the Supreme Court's *SAS* decision. Except as expressly admitted, Netlist denies the allegations in this paragraph.

335. Denied.

336. Denied.

337. Denied.

338. Denied.

339. Denied.

340. Denied.

341. Denied.

342. Denied.

343. Denied.

344. Denied.

345. Denied.

346. Denied.

347. Denied.

348. Denied.

349. Denied.

350. Denied.

351. Denied.

352. Denied.

353. Denied.

354. Denied.

355. Denied.

356. Denied.

357. Paragraph 357 purports to reference the content of the ’218 patent and the ’595 patent. The ’218 patent and the ’595 patents speak for themselves, and therefore a response is unnecessary. The allegations in this paragraph also state legal conclusions to which no response is required. Except as expressly admitted, Netlist denies the allegations of paragraph 357.

358. Denied.

359. Denied.

360. Denied.

361. Netlist admits that on March 21, 2019, the PTAB issued a Final Written Decision regarding the ’623 Patent. That decision speaks for itself. Except as expressly admitted, Netlist denies the allegations of paragraph 361.

362. Paragraph 362 purports to reference filings in connection with the prosecution of the ’218 and ’595 patents and these documents speak for themselves. Netlist incorporates its responses in paragraph 289. Netlist denies that it filed a terminal disclaimer for the ’623 patent over the ’837 patent and the application that issued as the ’218 patent. After the terminal disclaimer was filed in the ‘623 proceeding, the pending claims in U.S. Application No. 15/088,115

underwent several amendments before issuing as the '218 patent. Except as expressly admitted, Netlist denies the allegation and legal conclusions in this paragraph.

363. Denied.

364. Netlist is without knowledge sufficient to admit or deny the allegations in paragraph 364 and therefore, denies.

365. Denied. The Office allowed the '595 patent after being informed of the FWD for the '623 IPR.

366. Denied.

367. Denied.

368. Denied.

369. Denied.

COUNT X

Based on the Court's Order dismissing Count X, D.I. 38, no response is needed to paragraphs 370–403. To the extent further response is required, Netlist denies.

COUNT XI

Based on the Court's Order dismissing Count XI, D.I. 38, no response is needed to paragraphs 404–38. To the extent further response is required, Netlist denies.

COUNT XII

439. Netlist incorporates by reference its responses in the preceding paragraphs as if fully set forth herein.

440. Denied.

441. Netlist admits that it has submitted several Letters of Assurance. These letters speak for themselves, and no response is required. The remaining allegations in this paragraph

state a legal conclusion to which no response is required. To the extent any response is necessary, Netlist denies.

442. Given the Court's dismissal of the '912 patent, D.I. 38, no response is required. To the extent any response is necessary, Netlist denies.

443. Given the Court's dismissal of the '918 patent, D.I. 38, no response is required. To the extent any response is necessary, Netlist denies.

444. Given the Court's dismissal of the '019 application, D.I. 38, no response is required. To the extent any response is necessary, Netlist denies.

445. The allegations in this paragraph state a legal conclusion to which no response is required. To the extent any response is necessary, Netlist denies.

446. Denied.

447. Denied.

448. Netlist admits that it has taken the position that Samsung's license under the JDLA has been terminated. As to the remaining allegations in the paragraph, Netlist denies.

449. Given the Court's dismissal of the '912 patent, no response is required. To the extent any response is necessary, Netlist denies

450. Denied.

451. Denied.

JURY DEMAND

Netlist respectfully requests a trial by jury on all issues so triable.

PRAYER FOR RELIEF

Netlist denies that Plaintiffs are entitled to any relief and respectfully requests that the Court deny Plaintiffs' Prayer for Relief such that Plaintiffs shall take nothing in this action.

NETLIST INC.'S AFFIRMATIVE DEFENSES

Without assuming any burden that it would not otherwise bear under applicable law and rules, and specifically reserving its rights to assert additional affirmative defenses as further information or materials become available through discovery or otherwise, Netlist asserts the following affirmative defenses to the Complaint.

First Affirmative Defense: Lack of Subject Matter Jurisdiction

1. This Court lacks subject matter jurisdiction over Samsung's declaratory judgment and breach of contract claims.

Second Affirmative Defense: Failure to State a Claim

2. Samsung's FAC fails to state a claim upon which relief may be granted.

Third Affirmative Defense: Lack of Standing

3. Samsung lacks standing to seek the requested relief for a judgment declaring that SEC and SSI did not infringe Netlist's Patents-in-Suit.

Fourth Affirmative Defense: No Breach of Contract

4. Netlist has not breached any of its obligations, if any exist, under any of the agreements identified in Samsung's FAC.

Fifth Affirmative Defense: Breach of Contract by Samsung

5. Samsung cannot obtain relief pursuant to any agreements identified in the FAC because Samsung did not fulfill its obligation under these agreements.

6. Netlist and Samsung entered into the Joint Development and License Agreement ("JDLA") on November 12, 2015. Under the JDLA, Samsung received certain rights to Netlist's patents having an effective first filing date on or prior to the end of the capture period of the JDLA, *i.e.* five years beginning on November 12, 2015.

7. On July 15, 2020, Netlist sent a letter to Samsung terminating the JDLA due to Samsung's repeated breach of its contract obligations to supply the NAND and DRAM products to Netlist on Netlist's request and to reasonably cooperate with Netlist in any lawful efforts to claim a tax credit or refund or exemption with the tax withholding authorities. Netlist also filed a lawsuit against Samsung in the United States District Court for the Central District of California for breach of the JDLA. *Netlist, Inc. v. Samsung Elec. Co. Ltd.*, No. 20-cv-993-MCS (C.D. Cal.). On October 14, 2021, a Judge in the Central District of California found that there was no material factual dispute that Samsung had materially breached the JDLA and held that Netlist had properly terminated the agreement. *Id*. Dkt. 186. Samsung continued to manufacture, use, sell, offer to sell, and import to the United States the Accused Instrumentalities after the JDLA was terminated.

8. On October 15, 2020, after Netlist terminated the JDLA, Netlist sent a letter to SEC, asking SEC and its subsidiaries to engage in a formal licensing discussion with Netlist regarding Netlist's Patents-in-Suit. Samsung refused to engage in such discussions with Netlist.

9. As a result of Samsung's material breach of the JDLA and its failure to engage in licensing discussion with Netlist, Samsung is not entitled to receive a RAND license for Netlist's patents to the extent that they are essential to any JEDEC standards.

Sixth Affirmative Defense: Unclean Hands

10. Netlist incorporates by reference its Affirmative Defenses in the preceding paragraphs as if fully set forth herein.

11. Samsung's claims are barred in whole or in part by the doctrine of unclean hands.

Seventh Affirmative Defense: Estoppel

12. Netlist incorporates by reference its Affirmative Defenses in the preceding paragraphs as if fully set forth herein.

13. Samsung's claims are barred by the doctrine of estoppel.

Eighth Affirmative Defense: Limitation on Damages

14. Samsung has failed to take reasonable and necessary steps to avoid damages, if any, alleged in the FAC. To the extent such damages, if any, were incurred, Samsung's recovery, if any, should be reduced accordingly.

Reservation of Additional Defenses

15. Netlist reserves the right to assert additional defenses in the event that discovery or other analysis indicate that additional defenses are warranted.

WHEREFORE, Netlist respectfully requests that this Court dismiss the Complaint in its entirety, deny all relief Samsung requested therein, and award Netlist costs and expenses it has incurred and such further relief as the Court deems just and proper.

NETLIST INC.'S FIRST AMENDED COUNTERCLAIMS AND CROSSCLAIMS

For its counterclaims against Counter-Defendants Samsung Electronics Co., Ltd. ("SEC") and Samsung Semiconductor, Inc. ("SSI") (collectively "Samsung") and Cross-Defendants Google LLC and Alphabet Inc. ("Alphabet") (collectively, "Google"). Counter-Plaintiff Netlist, Inc. ("Netlist") alleges as follows upon actual knowledge with respect to Netlist and its own acts, and upon information and belief as to all other matters:

1. This Action involves Netlist's U.S. Patent Nos. 10,217,523 (the "'523 patent," Ex. 1), 9,858,218 (the "'218 patent," Ex. 2), and 10,474,595 (the "'595 patent," Ex. 3) (collectively "Netlists' Patents-in-Suit").

THE PARTIES

2. Counterplaintiff Netlist is a corporation organized and existing under the laws of the State of Delaware, having a principal place of business at 111 Academy Drive, Suite 100, Irvine, CA 92617.

3. Samsung contends that SEC is a corporation organized and existing under the laws of the Republic of Korea, with its principal place of business at 129 Samsung-ro, Yeongtong-gu, Suwon, Gyeonggi, 16677, Republic of Korea. On information and belief, SEC is the worldwide parent corporation for SSI, and is responsible for the infringing activities identified in this Counterclaims. On information and belief, SEC's Device Solutions division is involved in the design, manufacture, use, offering for sale and/or sales of certain semiconductor products, including the Accused Instrumentalities as defined below. On information and belief, SEC is also involved in the design, manufacture, and provision of products sold by SEC's subsidiaries or affiliates.

4. On information and belief, SSI is a corporation organized and existing under the laws of the State of California. On information and belief, SSI, collectively with SEC, operates the Device Solutions division, which is involved in the design, manufacture, use, offering for sale and/or sales of certain semiconductor products, including the Accused Instrumentalities as defined below.

5. On information and belief, Google LLC is a limited liability company organized and existing under the laws of the State of Delaware. On information and belief, Google LLC, individually and collectively with SEC, SSI, and Alphabet, is involved in the design, manufacture, purchase, use, offering for sale, sale, and/or importation to the United States of certain semiconductor products, including the Accused Instrumentalities as defined below. Google LLC has a registered agent to accept service of process within the State of Delaware located at 251 Little Falls Drive, Wilmington, DE 19808.

6. On information and belief, Alphabet is a corporation organized and existing under the laws of the State of Delaware. On information and belief, Alphabet is the ultimate parent company of Google LLC. On information and belief, Alphabet, individually and collectively with SEC, SSI, and Google LLC, is involved in the design, manufacture, purchase, use, offering for sale, sale, and/or importation to the United States of certain semiconductor products, including the Accused Instrumentalities as defined below. Alphabet has a registered agent to accept service of process within the State of Delaware located at 251 Little Falls Drive, Wilmington, DE 19808.

7. On information and belief, Defendants have used, sold, or offered to sell products and services, including the Accused Instrumentalities, in this judicial district.

JURISDICTION AND VENUE

8. Subject matter jurisdiction is based on 28 U.S.C. § 1338, in that this action arises under federal statute, the patent laws of the United States. 35 U.S.C. §§ 100, *et seq*.

9. SEC and SSI are both subject to this Court's personal jurisdiction because SEC and SSI have purposefully availed themselves of the benefits and protections of the courts in Delaware, including by bringing this instant lawsuit. This Court has jurisdiction over SEC and SSI also because they conduct business in Delaware and performed and continue to perform acts of infringement in this District.

10. Google LLC and Alphabet are subject to this Court's personal jurisdiction because they are organized under the laws of the State of Delaware and maintain a registered agent in Delaware.

11. Venue is proper in this District because SEC and SSI initiated this instant lawsuit in this District and Google LLC and Alphabet are organized under the laws of the State of Delaware. Venue is also proper as to SEC under 28 U.S.C. § 1391(c)(3) because SEC is a foreign entity incorporated under the laws of the Republic of Korea.

BACKGROUND

12. Since its founding in 2000, Netlist has been a leading innovator in high-performance memory module technologies. Netlist designs and manufactures a wide variety of high-performance products for the cloud computing, virtualization and high-performance computing markets. Netlist's technology enables users to derive useful information from vast amounts of data in a shorter period of time. These capabilities will become increasingly valuable as the volume of data continues to dramatically increase.

13. The technologies disclosed and claimed in the '523, '595, and '218 patents relate generally to memory modules. In many commercial products, a memory module is a printed circuit board that contains, among other components, a plurality of individual memory devices (such as DRAMs). The memory devices are typically arranged in "ranks," which are accessible by a processor or memory controller of the host system. A memory module is typically installed into a memory slot on a computer motherboard and serve as memory for computer systems.

14. Memory modules are designed for various purposes, including use in server computers supporting cloud-based computing and other data-intensive applications. The structure, function, and operation of memory modules are often defined, specified, and standardized by the JEDEC Solid State Technology Association ("JEDEC"), a standard-setting body for the microelectronics industry. Memory modules are typically characterized by the generation of DRAM on the module (*e.g.*, DDR5, DDR4, DDR3) and the type of module (*e.g.*, RDIMM, LRDIMM).

15. Dual in-line memory modules ("DIMMs") are a type of memory module which generally include SDRAMs mounted on a printed circuit board with other components, *e.g.*, serial presence detect ("SPD") and Hub with thermal sensors. Registered dual in-line memory modules ("RDIMMs") are a type of memory module that use a hardware register (e.g., registering clock driver, or "RCD") that buffers the address and command signals between each DRAM and the memory controller. Load-reduced dual in-line memory modules ("LRDIMMs") are a type of memory module that generally include SDRAMs mounted on a printed circuit board. LRDIMMs typically also include an RCD for transmitting control and address signals to the SDRAMs and data buffers between the host controller and memory devices.

16. Netlist designs and manufactures a wide variety of high-performance products for the cloud computing, virtualization, and high-performance computing markets. Netlist's technology enables users to derive useful information from vast amounts of data in a shorter period of time. These capabilities will become increasingly valuable as the volume of data continues to dramatically increase.

17. Netlist has a long history of being the first to market with disruptive new products such as the first LRDIMM, HyperCloud®, based on Netlist's distributed buffer architecture. Netlist's—and the industry's—first LRDIMM product demonstrated what was previously thought to be impossible: that a server could be fully loaded with memory and still operate at the highest system speeds available at the time.

18. Netlist was also the first to bring NAND flash to the memory channel with its NVvault® NVDIMM. These innovative products built on Netlist's early pioneering work in areas such as embedding passives into printed circuit boards to free up board real estate, doubling densities via quad-rank double data rate (DDR) technology, and other off-chip technology advances that resulted in improved performance and lower costs compared to conventional memory.

19. Netlist's innovative LRDIMM technology has since been adopted by JEDEC in its DDR4 LRDIMM standard that is used by companies throughout the industry.

The Asserted '523 Patent

20. The '523 patent, titled "Multi-Mode Memory Module with Data Handlers," issued to inventors Dr. Hyun Lee, Jayesh R. Bhakta, and Soonju Choi on February 26, 2019. The '523 patent is a continuation of U.S. patent application Ser. No. 13/745,790, filed Jan. 19, 2013, now U.S. Pat. No. 8,689,064 ("the '064 patent"), which is a continuation of U.S. patent application Ser.

No. 13/183,253, filed Jul. 14, 2011, now U.S. Pat. No. 8,359,501 ("the '501 patent"), which is a continuation of U.S. patent application Ser. No. 12/422,925, filed Apr. 13, 2009, now U.S. Pat. No. 8,001,434 ("the '434 patent").

21. Netlist owns by assignment all rights, title, and interest in and to the '523 patent.

22. The '523 patent relates to memory subsystems and, more specifically, a self-testing architecture for memory modules that utilizes certain on-board components to conduct testing functions "without substantial system memory controller involvement." Ex. 1 at 1:33-34. The '523 patent discloses a memory module that includes on-board logic to assist in the performance of self-testing functions, including a control module and data module that communicate with the memory devices on the module, as depicted in Figure 3 below.

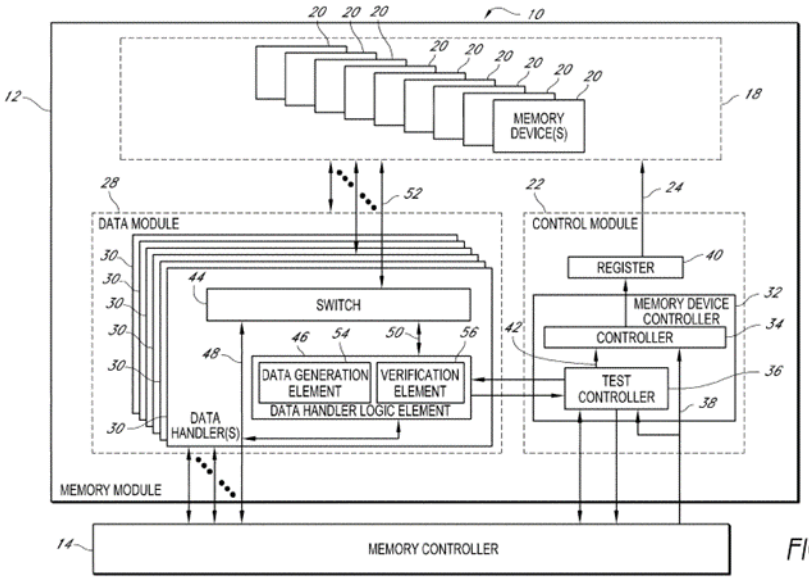


FIG. 3

23. The '523 patent discloses the use of at least two "modes" of operations for the memory module, including a "normal" operating mode and a "self-test" mode. In the first mode of operation, the data module propagates data signals between the system memory controller and the memory devices while the control module provides address and control signals based on the address and control signals from the system memory controller. In the second mode of operation,

the data modules isolate the respective memory devices from the system memory controller and generate data patterns that are sent to the memory devices while the control module generates the respective address and control signals.

The Asserted '595 Patent

24. The '595 patent, titled "Memory Module Having an Open-drain Output Pin for Parity Error in a First Mode and for Training Sequences in a Second Mode," issued to inventor Dr. Hyun Lee on November 12, 2019. The '595 patent issued from Application No. 15/857,553, filed on December 28, 2017. The '595 patent is a continuation of the '218 patent.

25. Netlist owns by assignment all rights, title, and interest in and to the '595 patent.

26. The '595 patent relates to memory modules that operate in two distinct modes, where the module performs memory read or write operations in one mode, and operations related to one or more training sequences in the other. Ex. 3 (the '595 patent). Similar to the '218 patent, the '595 patent provides a solution whereby the memory module may use existing hardware to signal the system memory controller during initialization/training, e.g., to "notify" the MCH when training is complete.

The Asserted '218 Patent

27. The '218 patent, titled "Memory Module and Methods for Handshaking with a Memory Controller," issued to inventor Dr. Hyun Lee on January 2, 2018. The '218 patent issued from Application No. 15/088,115, filed on April 1, 2016. The '218 patent is a continuation of application No. 13/942,721, filed on July 16, 2013, now U.S. Patent No. 9,311,116, which is a continuation of application No. 12/815,339, filed on June 14, 2010, now U.S. Patent No. 8,489,837 ("the '837 patent").

28. Netlist owns by assignment all rights, title, and interest in and to the '218 patent.

29. The ’218 patent relates to memory modules that operate in two distinct modes, where the module performs memory read or write operations in one mode, and one or more training sequences in the other.

30. As the ’218 patent explains, memory subsystems, “such as memory modules are generally involved in the initialization procedure for computer systems, including servers, personal computers, and the like.” Ex. 2 (the ’218 patent) at 1:25–27. However, at the time of the ’218 patent, “[e]xisting initialization schemes [had] certain inefficiencies which [led] to wasted time and expense,” *id.*, 2:49-50, in part because there was no existing method for a memory subsystem (e.g., memory module) to communicate to the memory controller hub (“MCH,” e.g., system memory controller) during initialization. *Id.*, 2:59-65. Prior art methods included the MCH “polling” the memory module to determine whether training was complete, or simply waiting a pre-determined period of time, based on an estimation of when the module controller would have completed the training sequence. *Id.*, 3:30-58. Both methods were inefficient because the system memory controller did not know when training was complete. *Id.*, 3:13-58.

31. The ’218 patent provides a solution whereby the memory module may use existing hardware to signal the system memory controller during initialization/training, e.g., to “notify” the MCH when training is complete. This was unprecedented because, prior to the invention, memory modules had always been reactive components, meaning that signals sent by a memory module were in response to a command or signals received from the host system. In contrast, the ’218 patent’s memory module is active, initiating contact with the host system by outputting to the host system a signal associated with training sequences. Such signaling can be an open drain signaling from the memory subsystem controller to the MCH and uses an open-drain output that already exists on the memory module.

32. The '218 patent memory modules can have both a "first mode" and a "second mode." In the first mode, the memory module executes training and is not accessed by the host for read or write operations. In the second mode, the memory module performs standard operations (e.g., read or write operations) in response to read or write commands from the host system.

Samsung's and Google's Infringing Activities

33. Samsung is a global technology company and one of the largest manufacturers of semiconductor memory products such as DRAM, NAND Flash, and MCP (Multi-Chip Package). Samsung develops, manufactures, sells, offers to sell, and imports into the United States memory components and memory modules designed for, among other things, use in servers such as those supporting cloud-based computing and other data-intensive applications.

34. On information and belief, Samsung makes, uses, sells, offers to sell, and/or imports within this District and elsewhere in the United States, without authority, infringing DDR4 RDIMMs products and other products that have materially the same structures and designs in relevant parts ("the accused DDR4 RDIMMs") and infringing DDR4 LRDIMMs products and other products that have materially the same structures and designs in relevant parts ("the accused DDR4 LRDIMMs") (collectively the "Accused Instrumentalities").

35. By way of example, the Accused Instrumentalities include, but are not limited to, Samsung products listed on Samsung's module-selector web page. *Memory Modules For Extensive Use*, Samsung, https://www.samsung.com/semiconductor/dram/module.

36. Netlist and Samsung entered into a Joint Development and License Agreement ("JDLA") on November 12, 2015. Under the JDLA, Samsung received certain rights to certain of

Netlist's patents having an effective first filing date on or prior to the end of the capture period of the JDLA, *i.e.* five years beginning on November 12, 2015.

37. On July 15, 2020, Netlist sent a letter to Samsung terminating the JDLA due to Samsung's repeated breach of its contract obligations to supply NAND and DRAM products to Netlist on Netlist's request and to reasonably cooperate with Netlist in any lawful efforts to claim a tax credit or refund or exemption with the tax withholding authorities. Netlist filed a lawsuit against Samsung in the United States District Court for the Central District of California for breach of the JDLA. *Netlist, Inc. v. Samsung Elec. Co. Ltd.*, No. 20-cv-993 (C.D. Cal.).

38. On October 14, 2021, the Central District of California found that there was no material factual dispute that Samsung had materially breached the JDLA and held that Netlist had properly terminated the agreement. *Id*. Dkt. 186. A final judgment finding the same was entered against Samsung on February 15, 2022. *Id.* Dkt. 306. Samsung continued to manufacture, use, sell, offer to sell, and import to the United States the Accused Instrumentalities after the JDLA was terminated.

39. Google is a global technology company and the largest provider of search engine services in the world, including searches through Google.com and YouTube.com. On information and belief, Google provides an expansive range of services including cloud computing, data storage, quantum computing, artificial intelligence, and machine learning. On information and belief, Google is one of the largest users of server computers and memory modules worldwide, and it develops, manufactures, purchases, uses, and/or imports into the United States memory components and memory modules designed for, among other things, use in Google's and its affiliates' server computers and other data-intensive applications.

40. On information and belief, Google makes, uses, sells, offers to sell, and/or imports within this District and elsewhere in the United States the Accused Instrumentalities without authority. On information and belief, Google has employed third party vendors to make, assemble, import, or export the Accused Instrumentalities without authority.

41. On information and belief, Samsung is one of the suppliers of the Accused Instrumentalities used by Google, including but not limited to Samsung products listed on Samsung's module-selector web page. *Memory Modules For Extensive Use*, Samsung, https://www.samsung.com/semiconductor/dram/module.

42. On information and belief, Samsung and Google are parties to indemnification agreement(s) in connection with the Accused Instrumentalities Samsung supplied to Google.

CLAIMS FOR RELIEF

Count I

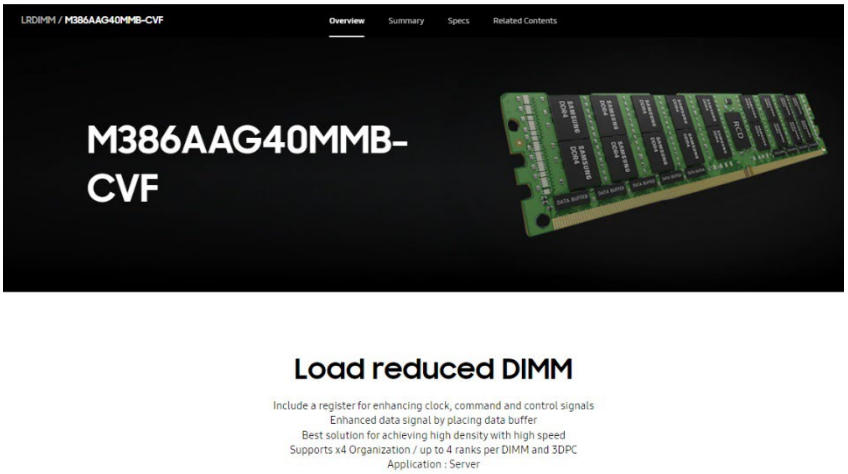
(Infringement of the '523 Patent)

43. Netlist alleges and incorporates by reference the allegations of the preceding paragraphs of the Affirmative Defenses, Counterclaims, and Cross-claims as if fully set forth herein.

44. On information and belief, Samsung and Google directly infringed and are currently infringing at least one claim of the '523 patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the accused DDR4 LRDIMMs and other products with materially the same structures in relevant parts. For example, and as shown below, the accused DDR4 LRDIMMs and

other products with materially the same structures in relevant parts infringe at least claim 1 of the '523 patent.[1]

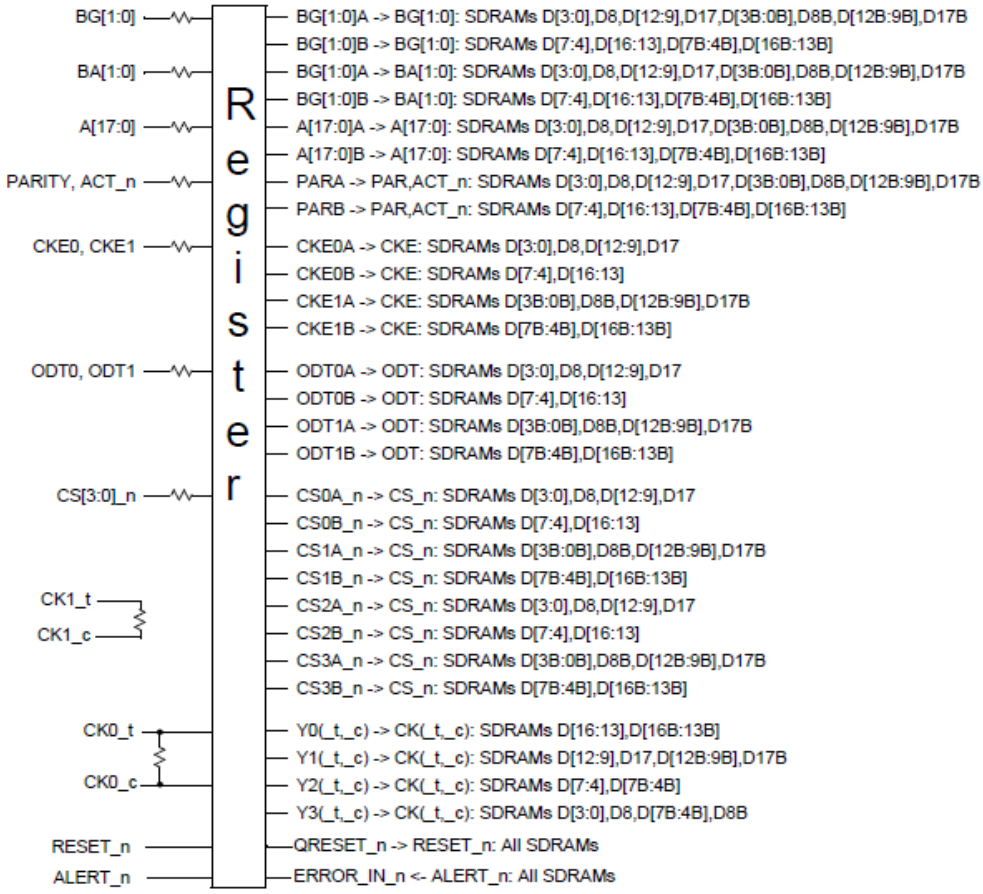
45. To the extent the preamble is limiting, on information and belief, each accused DDR4 LRDIMM comprises a memory module operable to communicate with a memory controller via a memory bus. As an example, Samsung's website markets and contains datasheets for the accused DDR4 LRDIMMs:

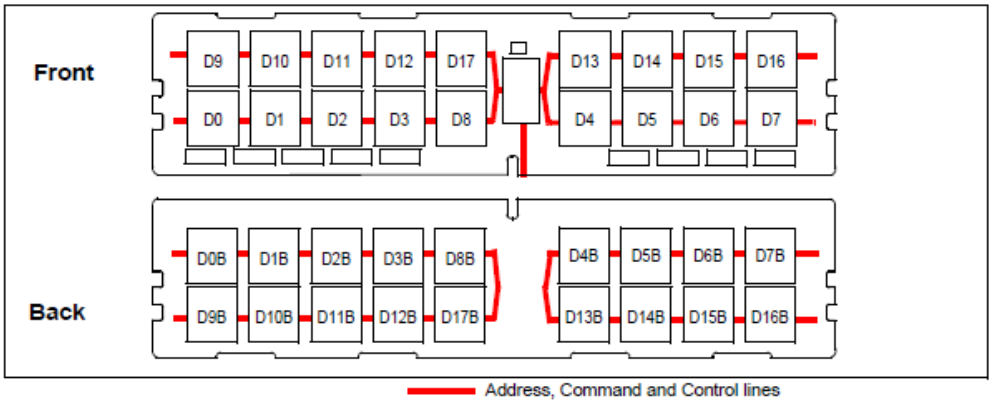


Ex. 4 at 2 (depiction of Samsung DDR4 LRDIMM M386AAG40MMB).

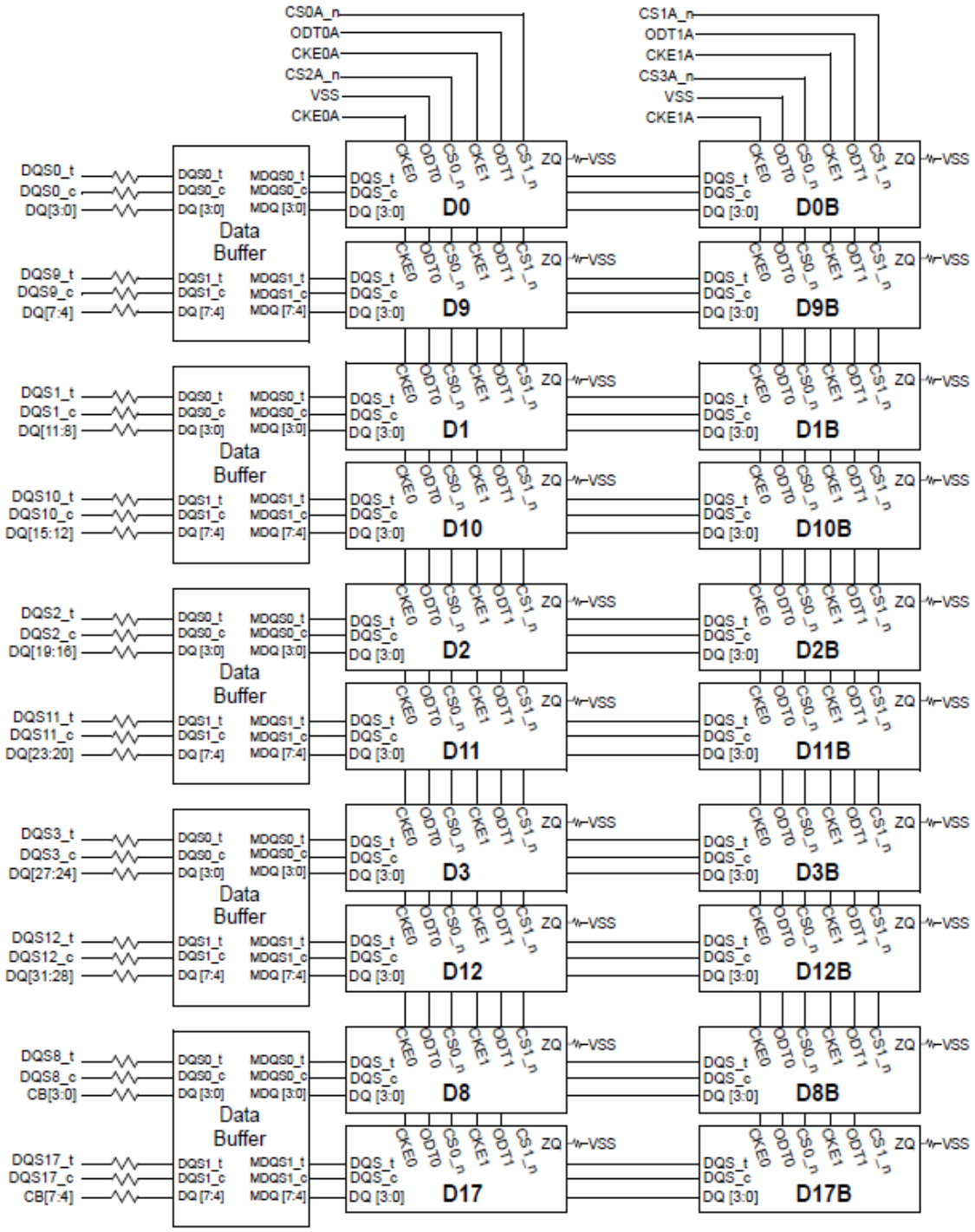
[1] The theories set forth herein are based on Netlist's present understanding of Samsung's and Google's Accused Instrumentalities. Netlist reserves the right to supplement or amend these contentions as permitted by the Local Rules and any Orders of the Court as discovery progresses. Further, Netlist's contentions contain images and examples illustrating Netlist's infringement theories. As such, the images and examples are not intended, and should not be read, as narrowing or limiting the scope of these contentions.

46. On information and belief, the accused DDR4 LRDIMMs each comprises memory devices mounted on a circuit board and the memory devices have address and control ports and data ports, as shown below:





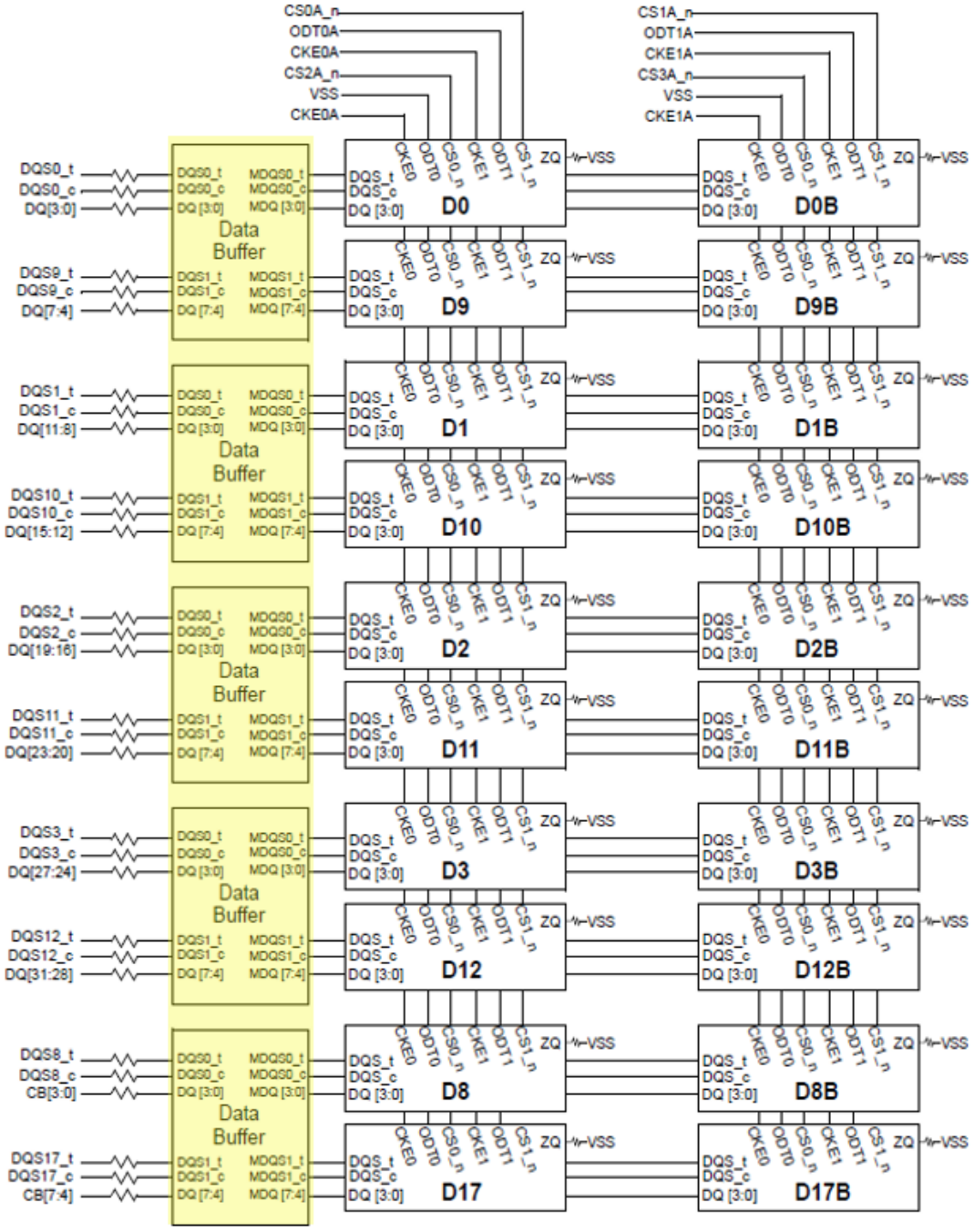
Ex. 5 at 11 (Datasheets for M386AAG40MMB).



Ex. 5 at 12 (Datasheets for M386AAG40MMB) (showing the memory devices D0, D1, D2 . . . D17, D17B; address/control ports CS0 . . . CS1 . . . CS2 . . . ; data ports DQ, DQS . . .).

47. On information and belief, the accused DDR4 LRDIMMs further each comprises a data module that includes data handler logic elements. The data module is mounted on the circuit

board and coupled between the data ports of the memory devices and the system memory bus. For example, the figure below shows data buffers on the accused DDR4 LRDIMMs, i.e., the data handler logic elements:



Ex. 5 at 12 (Datasheets for M386AAG40MMB). The diagram below shows the logic element(s):

4.61 Logic Diagram

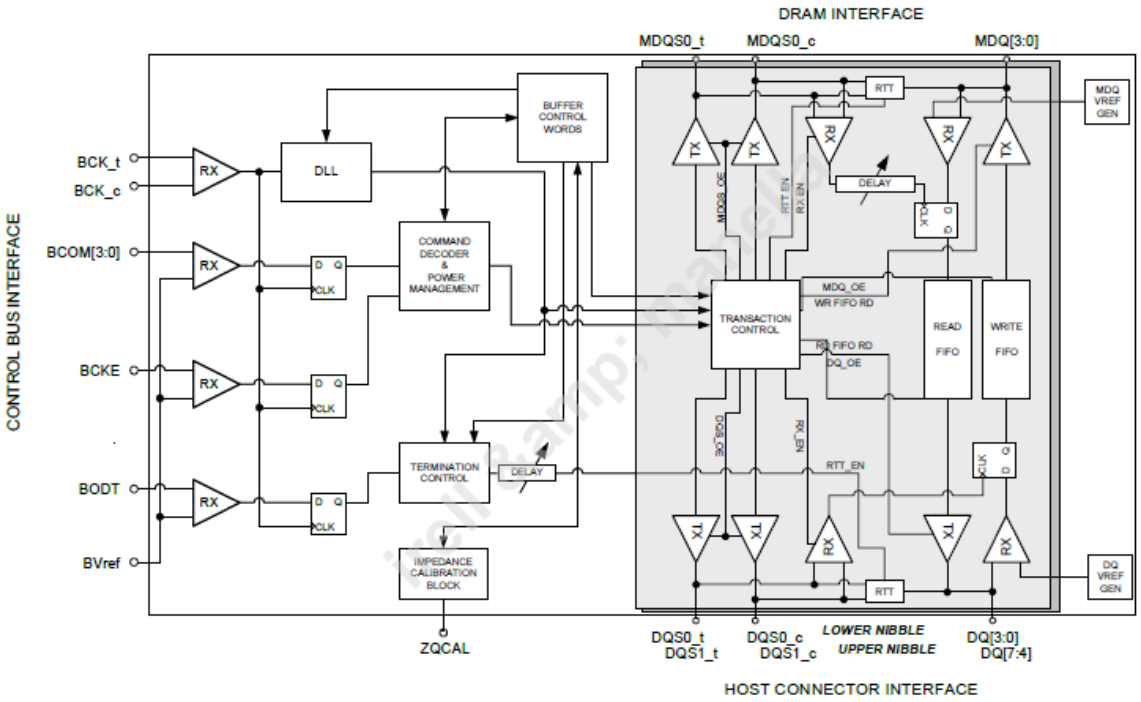
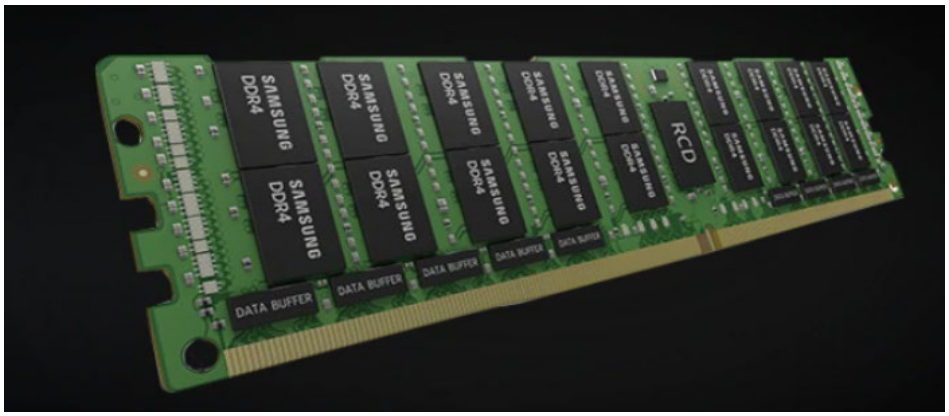


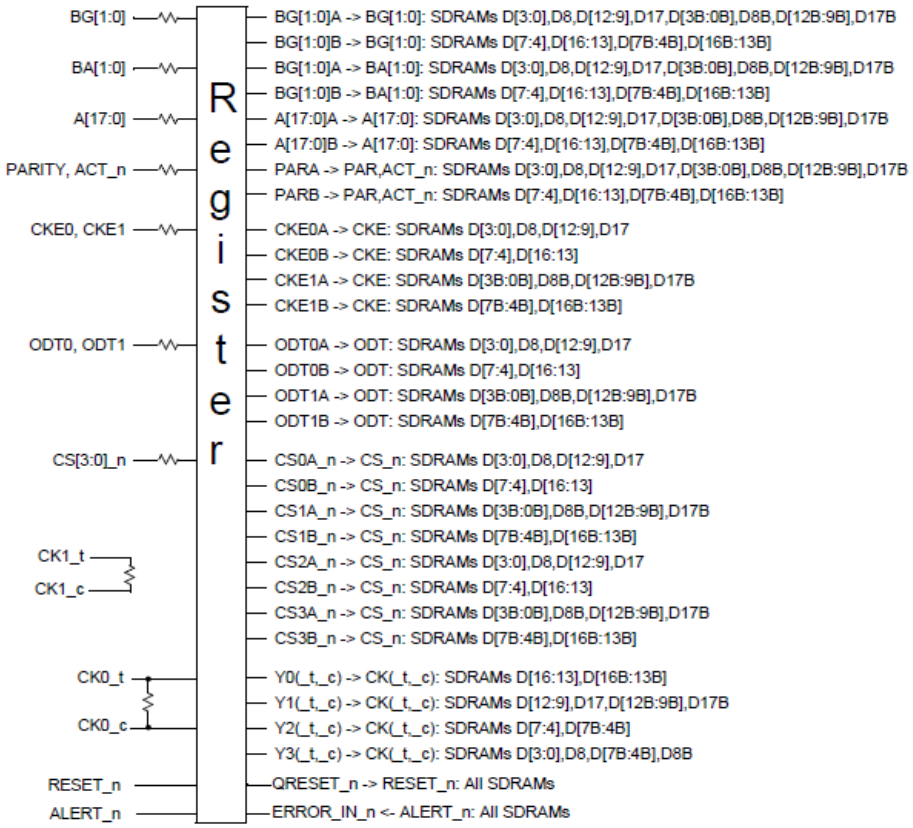
Figure 15 — Logic Diagram

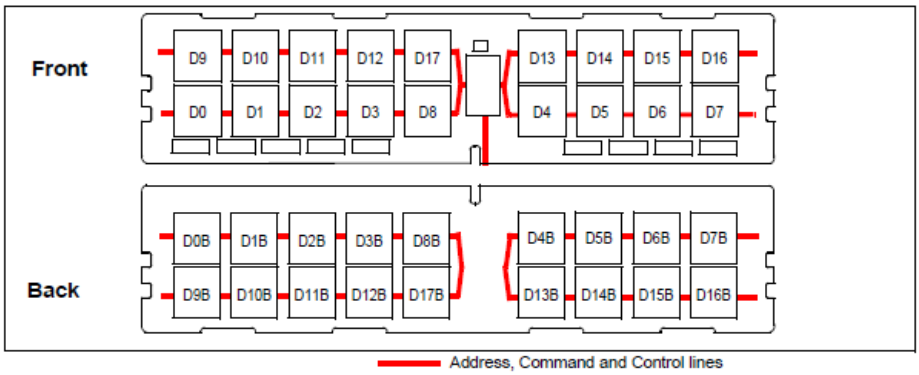
Ex. 6, Fig. 15 (excerpts for JESD82-32A).

48. On information and belief, the accused DDR4 LRDIMMs each comprises a control module mounted on the circuit board and coupled to the data module, the address and control ports of the memory devices, and the system memory bus. For example, on information and belief, the accused DDR4 LRDIMMs contain a JEDEC standard-compliant RCD on the circuit board.



Ex. 4 (M386AAG40MMB).



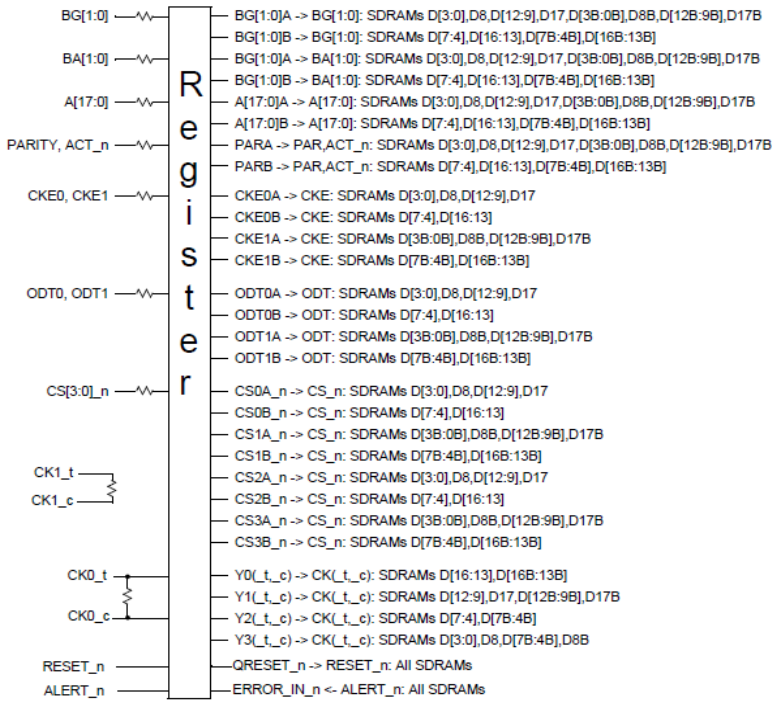


Ex. 5 at 11 (Datasheets for M386AAG40MMB) (showing the RCD).

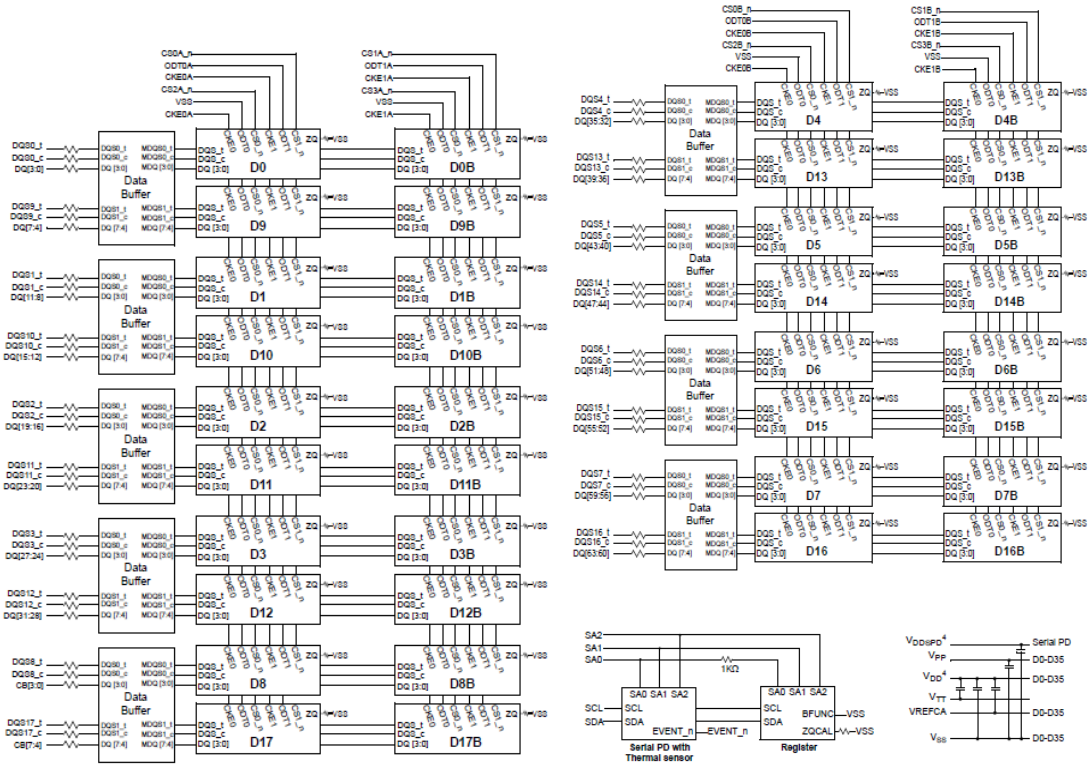
49. On information and belief, Samsung's and Google's accused DDR4 LRDIMMs are operable in two modes—the normal operating mode and the DB-to-DRAM Write Delay ("MWD") Training mode.

50. On information and belief, in the first mode, the control module is configured to receive system address and control signals from the system memory controller and to output first

memory address and control signals to the memory devices according to the system address and control signals. The data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller. For example, the figures below indicate the operation of Samsung's and Google's accused DDR4 LRDIMMs under the first mode:



Ex. 5 at 11 (Datasheets for M386AAG40MMB) (showing the RCD).



Ex. 5 at 12-13 (Datasheets for M386AAG40MMB).

As shown in the JEDEC standards figures below, on information and belief, the RCD in the accused DDR4 LRDIMMs is configured to receive a set of input address/control signals corresponding to a memory read or write command information (*e.g.*, CS, A0-A17, ACT, RAS, CAS, WE, CKE, etc.) from the memory controller:

6.1 Signal Groups

This specification categorizes DDR4 SDRAM timing-critical signals into seven groups. Figure 3 summarizes the signals contained in each group. All signal groups, except Data, implement a fly-by topology. The signal groups are:

1. DQ and DQS signals connector to Data Buffer (DB)
2. DQ and DQS signals DB to SDRAM
3. PreRegister ADD/CMD and CTRL
4. PreRegister CK
5. PostRegister ADD/CMD
6. PostRegister Control
7. PostRegister CK
8. PostRegister BCOM, BODT, BCKE
9. PostRegister BCK

The PreRegister ADD/CMD and CTRL group includes A0-A17, BA0-BA1, BG0-BG1, C0-C2, PARITY, CSx_n, CKEx, and ODTx.

The PostRegister ADD/CMD group includes A0-A17, BA0-BA1, BG0-BG1, C0-C2, and PARITY.

The PostRegister CTRL group includes CSx_n, CKEx, and ODTx.

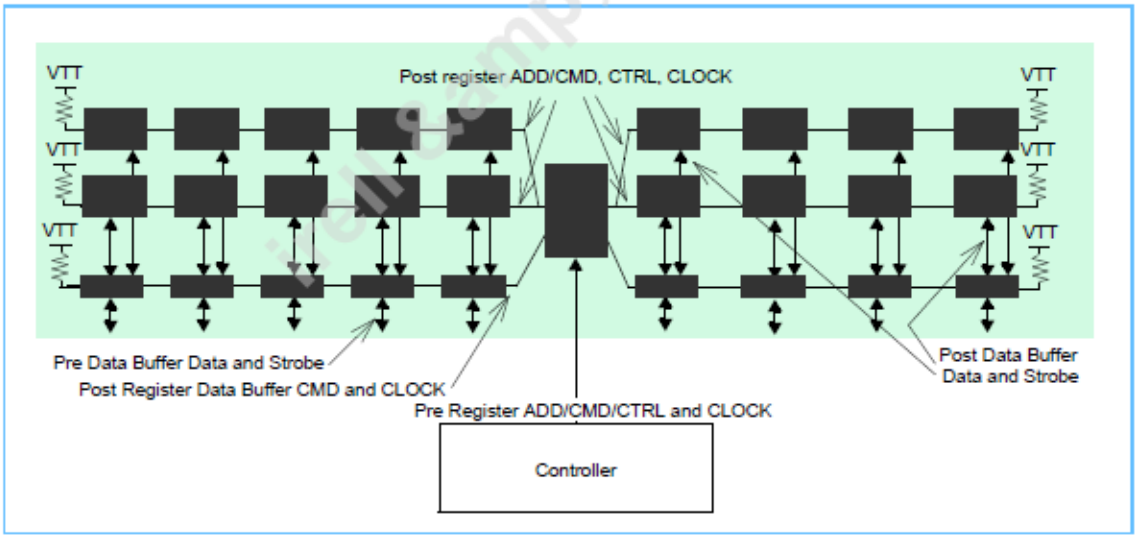


Figure 3 — LRDIMM Topologies

Ex. 10 at 17 (excerpts for JEDEC Standard No. 21C).

Table 4 — Input/Output Functional Description

Symbol	Type	Function
CK0_t, CK0_c, CK1_t, CK1_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT, and CKE, are disabled during power-down. Input buffer, excluding CKE, are disabled during Self-Refresh.
CS0_n, CS1_n, CS2_n, CS3_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection. CS_n is considered part of the command code.
C0, C1, C2	Input	Chip ID: Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODT0, ODT1	Input	On-Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 will be considered as Row Address A16, A15, and A14
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n) define the command being entered. These pins are multi-function. For example, for activation with ACT_n Low, the pins are Addresses A16, A15, and A14, but for non-activation commands with ACT_n High, these are Command pins for Read, Write, and other commands defined in the command truth table
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write, or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle.
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write, or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15, and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for 16 Gb x4 SDRAM configurations.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	CMOS Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and Inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register, then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor-specific data sheets to determine which DQ is used.

Ex. 10 at 8 & Table 4 (excerpts for JEDEC Standard No. 21C).

2.22 Logic diagram

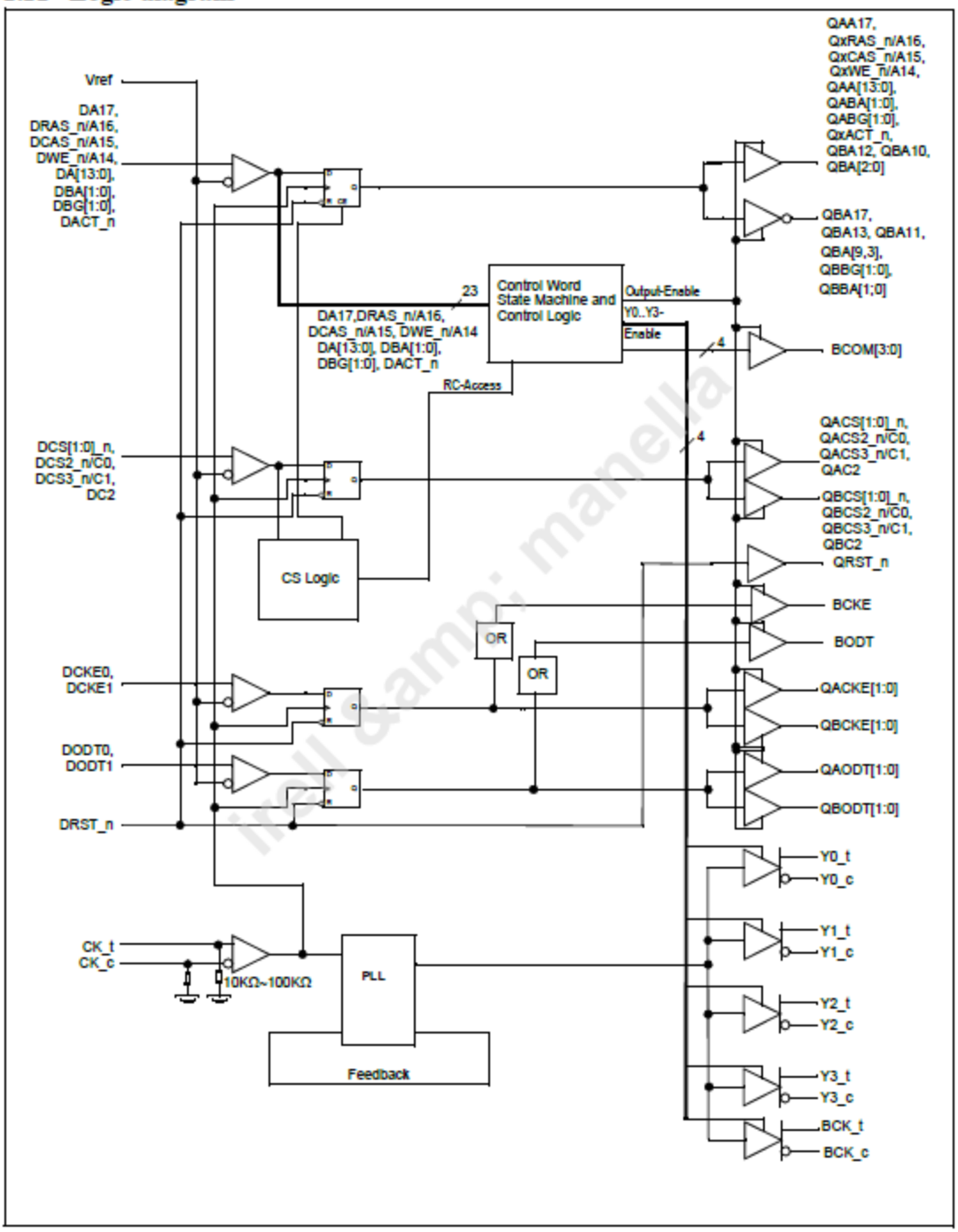


Figure 28 — Logic diagram (positive logic)

Ex. 9 at 66 (excerpts for JESD82-31A).

51. On information and belief, the first data signals are transmitted or received by the memory devices in response to read or write commands, respectively.

2.21.1 Terminal Functions Function tables

Table 21 — Terminal functions

Signal Group	Signal Name	Type	Description
Input Control bus	DCKE0/1 DODT0/1	CMOS[1] V_{REF} based	DRAM corresponding register function pins not associated with Chip Select.
	DCS0_n..DCS1_n	CMOS[1] V_{REF} based	DRAM corresponding register Chip Select signals.
	DCS2_n..DCS3_n or DC0..DC1	CMOS[1] V_{REF} based	DRAM corresponding register Chip Select signals. These pins initiate DRAM address/command decodes,. Some of these have alternative functions: • DCS2_n <=> DC0 • DCS3_n <=> DC1
	DC2	CMOS[1] V_{REF} based	DRAM corresponding register Chip ID 2 signal.
Input Address and Command bus	DA0..DA13, DA17 DBA0..DBA1, DBG0..DBG1	CMOS[1] V_{REF} based	DRAM corresponding register inputs.
	DA14..DA16 or DWE_n, DCAS_n, DRAS_n	CMOS[1] V_{REF} based	DRAM corresponding register inputs. In case of an ACT command some of these terminals have an alternative function: DRAM corresponding register command signals. • DA14 <=> DWE_n • DA15 <=> DCAS_n • DA16 <=> DRAS_n
	DACT_n	CMOS[1] V_{REF} based	DRAM corresponding register DACT_n signal.
Clock inputs	CK_t/CK_c	CMOS differential	Differential master clock input pair to the PLL with a 10 KΩ ~ 100 KΩ pull-down resistor.
Reset input	DRST_n	CMOS input	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float.
Parity input	DPAR	CMOS[1] V_{REF} based	Input parity is received on pin DPAR and should maintain even parity across the address and command inputs (see above), at the rising edge of the input clock.
Error input	ERROR_IN_n	Low voltage swing CMOS input	DRAM address parity and CRC ALERT_n output is connected to this input pin, which in turn is buffered and redriven to the ALERT_n output of the register. Requires external pull up resistor. In LRDIMM applications, the DB ALERT_n outputs are also connected to this input.
Data buffer control and communication outputs	BODT	CMOS[2]	Data buffer on-die termination signal
	BCKE	CMOS[2]	Data buffer clock enable signal for PLL power management
	BCOM[3:0]	CMOS[2]	Register communication bus for data buffer programming and control access
	BCK_t/BCK_c	CMOS[2] differential	Differential clock output pair to the data buffer.
	BVrefCA	$V_{DD}/2$	Output reference voltage for data buffer control bus receivers

Table 21 — Terminal functions

Signal Group	Signal Name	Type	Description
Output Control bus	QACKE0/1, QAODT0/1, QBCKE0/1, QBODT0/1	CMOS[2]	Register output CKE and ODT signals.
	QACS0_n..QACS1_n, QBCS0_n..QBCS1_n	CMOS[2]	Register output Chip Select signals.
	QACS2_n..QACS3_n, QBCS2_n..QBCS3_n or QAC0..QAC1, QBC0..QBC1	CMOS[2]	Register output Chip Select signals. These pins initiate DRAM address/command decodes. Some of these have alternative functions: • QxCS2_n <=> QxC0 • QxCS3_n <=> QxC1
	QAC2, QBC2	CMOS[2]	Register output Chip ID2 signals.
Output Address and Command bus	QAA0..QAA13, QAA17, QBA0..QBA13, QBA17, QABA0..QABA1, QBBA0..QBBA1, QAG0..QAG1, QBG0..QBG1	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
	QAA14..QAA16, QBA14..QBA16 or QAWE_n, QACAS_n, QARAS_n, QBWE_n, QBCAS_n, QBRAS_n	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. In case of an ACT command some of these terminals have an alternative function: Register output command signals. • QxA14 <=> QxWE_n • QxA15 <=> QxCAS_n • QxA16 <=> QxRAS_n
	QAACT_n, QBACT_n	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
Vref output	QVrefCA	$V_{DD}/2$	Output reference voltage for DRAM receivers
Clock outputs	Y0_t..Y3_t, Y0_c..Y3_c or Y0_t, Y1_t, LCOM1, LCK_t Y0_c, Y1_c, LCOM0, LCK_c	CMOS[2] differential	Redriven clock for RDIMM and LRDIMM These pins have alternative functions for optional NVDIMM support. • Y2_t <=> LCOM1 (bidirectional pin) • Y2_c <=> LCOM0 (bidirectional pin) • Y3_t <=> LCK_t (input pin) • Y3_c <=> LCK_c (input pin)
RFU2	RFU2 or LCKE	CMOS[2]	Reserved for RDIMM and LRDIMM This pins has an alternative fuction for optional NVDIMM support. • RFU2 <=> LCKE (input pin)
RFU3	RFU3 or LCOM2	CMOS[2]	Reserved for RDIMM and LRDIMM This pins has an alternative function for optional NVDIMM support. • RFU3 <=> LCOM2 (input pin)
Reset output	QRST_n	CMOS[2]	Redriven reset. This is an asynchronous output. It is the responsibility of the DDR4RCD02 QRST_n to reset the DDR4 SDRAM on all DIMM topologies.
Parity outputs	QAPAR QBPAR	CMOS[2]	Redriven parity[3]
Error out	ALERT_n	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs when parity checking is enabled or that the ERROR_IN_n input was asserted, regardless of whether parity checking is enabled or not.

Table 21 — Terminal functions

Signal Group	Signal Name	Type	Description
I^2C Bus pins	SDA	Open drain I/O	I^2C Bus Data
	SCL	CMOS input[4]	I^2C Bus Clock
	SA[2:0]	CMOS input[4]	I^2C Bus Address signals
	BFUNC	CMOS input[5]	Function pin. BFUNC=V_{SS} for primary register, BFUNC=V_{DD} for secondary register
	V_{DDSPD}	Power input	I^2C Bus power input
Miscellaneous pins	VrefCA	$V_{DD}/2$	Input reference voltage for the CMOS inputs.
	V_{DD}	Power Input	Power supply voltage
	V_{SS}	Ground Input	Ground
	AV_{DD}	Analog Power	Analog supply voltage
	AV_{SS}	Analog Ground	Analog ground
	PV_{DD}	Clock Driver Output Power	Clock logic and clock output driver power supply
	PV_{SS}	Clock Driver Output Ground	Clock logic and clock output driver ground
	ZQCAL	Reference	Reference pin for driver calibration
	NU	Mechanical ball	Do not connect on PCB
	RFU[3:0]	I/O	Reserved for future use pins, must be left floating on DIMM and in DDR4RCD02

1. These receivers use internal or external VrefCA as the switching point reference.
2. These outputs with rail to rail signal swing and programmable impedance are optimized for memory applications to drive DRAM inputs over a terminated transmission line.
3. QBPAR will be inverted relative to DPAR if the device is configured with a parity calculation field = 00 in the Parity Control Word.
4. These inputs are 2.5 V inputs
5. This input is a 1.2 V input

Ex. 9 at 61-63 (excerpts for JESD82-31A).

4.61 Logic Diagram

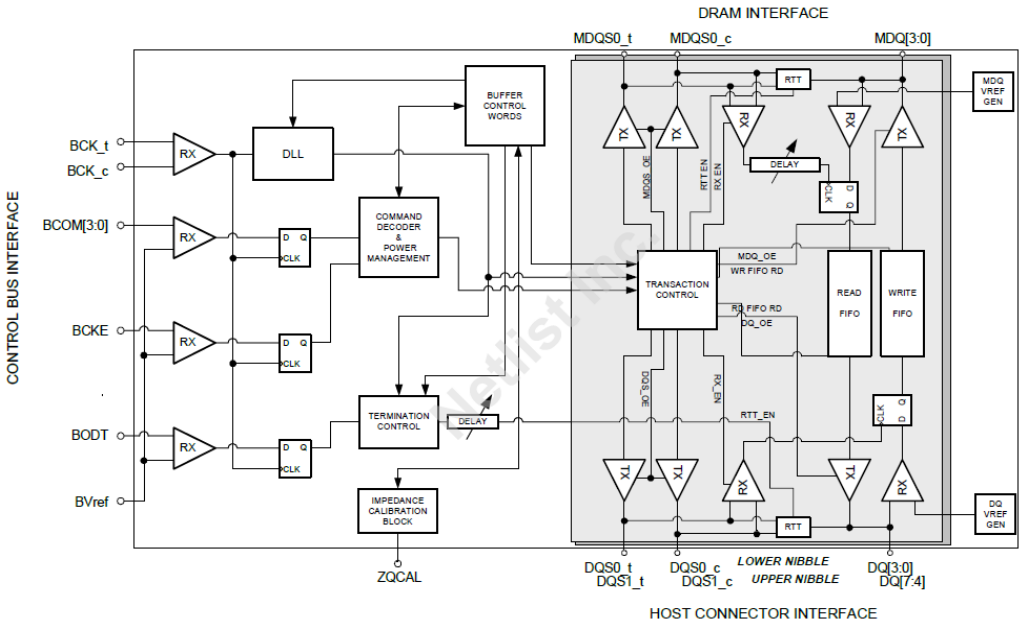


Figure 15 — Logic Diagram

Ex. 6, Fig. 15 (excerpts for JEDEC JESD82-32A).

52. On information and belief, in the second mode, the control module of Samsung/Google accused DDR4 LRDIMMs is configured to output second memory address and control signals to the address and control ports of the memory devices. For example, on information and belief, the accused DDR4 LRDIMMs contain a control module configured to operate in the DB-to-DRAM Write Delay ("MWD") Training Mode as described below:

2.20.5 DB-to-DRAM Write Delay (MWD) Training Mode

For the DB-to-DRAM write delay training, the MDQ-MDQS delay adjustments are performed in the data buffer so that the DRAM receives the MDQ and MDQS signals with the optimal phase relationship. The host-to-DB data path has not been trained at this time so the data that is written to the DRAM comes from the data buffer's internal data control words that are written through the DDR4 register via the BCOM bus. Since the DB to DRAM write training requires reading back the data for correctness it is performed after the DRAM to DB read training has already been finished.

To perform DB-to-DRAM write training, the host will first enable the MDQ-MDQS write delay training mode in the Training Mode Control Word (BC0C) and it will also program the MPRs F5BC0x through F5BC3x and F6BC0x through F6BC3x. After that the host sends write commands to an arbitrary DRAM location without driving data on the host interface. The data for these write commands come from the DB MPRs.

MPRx[7:0] is driven to MDQ[7:0], UIx, i.e. the content of MPR0 is driven out first and the content of MPR7 is driven out last.

To check whether the writes were successful, the host reads the data back from the same DRAM location and the data buffer performs a bit wise comparison with the data in the MPRs. If the data pattern is matched, the DQ pins are driven to '1' until the next comparison takes place or until the training mode is disabled. If the data pattern is not matched, the DQ pins are driven to '0'. In addition to driving the DQ pins, status for the MRD training mode is also provided in the Buffer Training Status word (F6BC5x). The status provided in F6BC5x can be modified by the Buffer Training Configuration control word (F6BC4x).

The phase relationship between the DRAM interface data strobe signals (MDQSx_t/MDQSx_c) and their corresponding data signals (MDQx) during write transactions is selected by buffer control words F[3:0]BC8x and F[3:0]BC9x for lower and upper nibble respectively. Since the DDR4DB02 uses the RANK ID fields in the BCOM Write Command and Read Command sequences to select the correct DRAM interface write leveling and DRAM interface receive enable timings for Writes and Reads respectively, the content of BC08 DA[1:0] is don't care while in this training mode. The nominal setting for F[3:0]BC8x/F[3:0]BC9x is one quarter of a cycle delay. The host controller may need to perform additional iterations of the training procedures, including DWL (DRAM Interface Write Leveling) and HWL (Host Interface Write Leveling) when non-default settings are written into F[3:0]BC8x/ F[3:0]BC9x.

For higher DDR4 data rates, fine adjustment of the phase of individual bit lanes relative to MDQS may be required. For this purpose the host controller can utilize the per lane MDQ-MDQS write delay control words F[7:4]BCCx through F[7:4]BCFx. F4BCCx controls the phase of bits MDQ0 and MDQ4 within the lower and upper nibble respectively for Rank 0, F5BCDx controls the phase bits MDQ1 and MDQ5 for Rank 1, and so on. Since all bits within a nibble a generally aligned by routing, only a small range of +/- 3 * 1/64 * t_{CK} is provided for fine-grained adjustment of individual bit lane delay differences. A negative delay in these control words means that the particular data lane requires slightly less delay than the previously established MDQ delay in F[3:0]BC8x or F[3:0]BC9x for the entire nibble. A positive delay in these control words means that the particular data lane requires slightly more delay than the previously established MDQ delay in F[3:0]BC8x or F[3:0]BC9x for the entire nibble.

To exit this training mode, the host controller can go back to resume normal operation or enable other training modes with a BCW to BC0C.

Ex. 6 at 33 (excerpts for JESD82-32A).

2.21.1 Terminal Functions Function tables

Table 21 — Terminal functions

Signal Group	Signal Name	Type	Description
Input Control bus	DCKE0/1 DODT0/1	CMOS[1] V_{REF} based	DRAM corresponding register function pins not associated with Chip Select.
	DCS0_n..DCS1_n	CMOS[1] V_{REF} based	DRAM corresponding register Chip Select signals.
	DCS2_n..DCS3_n or DC0..DC1	CMOS[1] V_{REF} based	DRAM corresponding register Chip Select signals. These pins initiate DRAM address/command decodes,. Some of these have alternative functions: • DCS2_n <=> DC0 • DCS3_n <=> DC1
	DC2	CMOS[1] V_{REF} based	DRAM corresponding register Chip ID 2 signal.
Input Address and Command bus	DA0..DA13, DA17 DBA0..DBA1, DBG0..DBG1	CMOS[1] V_{REF} based	DRAM corresponding register inputs.
	DA14..DA16 or DWE_n, DCAS_n, DRAS_n	CMOS[1] V_{REF} based	DRAM corresponding register inputs. In case of an ACT command some of these terminals have an alternative function: DRAM corresponding register command signals. • DA14 <=> DWE_n • DA15 <=> DCAS_n • DA16 <=> DRAS_n
	DACT_n	CMOS[1] V_{REF} based	DRAM corresponding register DACT_n signal.
Clock inputs	CK_t/CK_c	CMOS differential	Differential master clock input pair to the PLL with a 10 KΩ ~ 100 KΩ pull-down resistor.
Reset input	DRST_n	CMOS input	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float.
Parity input	DPAR	CMOS[1] V_{REF} based	Input parity is received on pin DPAR and should maintain even parity across the address and command inputs (see above), at the rising edge of the input clock.
Error input	ERROR_IN_n	Low voltage swing CMOS input	DRAM address parity and CRC ALERT_n output is connected to this input pin, which in turn is buffered and redriven to the ALERT_n output of the register. Requires external pull up resistor. In LRDIMM applications, the DB ALERT_n outputs are also connected to this input.
Data buffer control and communication outputs	BODT	CMOS[2]	Data buffer on-die termination signal
	BCKE	CMOS[2]	Data buffer clock enable signal for PLL power management
	BCOM[3:0]	CMOS[2]	Register communication bus for data buffer programming and control access
	BCK_t/BCK_c	CMOS[2] differential	Differential clock output pair to the data buffer.
	BVrefCA	$V_{DD}/2$	Output reference voltage for data buffer control bus receivers

Table 21 — Terminal functions

Signal Group	Signal Name	Type	Description
Output Control bus	QACKE0/1, QAODT0/1, QBCKE0/1, QBODT0/1	CMOS[2]	Register output CKE and ODT signals.
	QACS0_n..QACS1_n, QBCS0_n..QBCS1_n	CMOS[2]	Register output Chip Select signals.
	QACS2_n..QACS3_n, QBCS2_n..QBCS3_n or QAC0..QAC1, QBC0..QBC1	CMOS[2]	Register output Chip Select signals. These pins initiate DRAM address/command decodes. Some of these have alternative functions: • QxCS2_n <=> QxC0 • QxCS3_n <=> QxC1
	QAC2, QBC2	CMOS[2]	Register output Chip ID2 signals.
Output Address and Command bus	QAA0..QAA13, QAA17, QBA0..QBA13, QBA17, QABA0..QABA1, QBBA0..QBBA1, QAG0..QAG1, QBG0..QBG1	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
	QAA14..QAA16, QBA14..QBA16 or QAWE_n, QACAS_n, QARAS_n, QBWE_n, QBCAS_n, QBRAS_n	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. In case of an ACT command some of these terminals have an alternative function: Register output command signals. • QxA14 <=> QxWE_n • QxA15 <=> QxCAS_n • QxA16 <=> QxRAS_n
	QAACT_n, QBACT_n	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
Vref output	QVrefCA	$V_{DD}/2$	Output reference voltage for DRAM receivers
Clock outputs	Y0_t..Y3_t, Y0_c..Y3_c or Y0_t, Y1_t, LCOM1, LCK_t Y0_c, Y1_c, LCOM0, LCK_c	CMOS[2] differential	Redriven clock for RDIMM and LRDIMM These pins have alternative functions for optional NVDIMM support. • Y2_t <=> LCOM1 (bidirectional pin) • Y2_c <=> LCOM0 (bidirectional pin) • Y3_t <=> LCK_t (input pin) • Y3_c <=> LCK_c (input pin)
RFU2	RFU2 or LCKE	CMOS[2]	Reserved for RDIMM and LRDIMM This pins has an alternative fuction for optional NVDIMM support. • RFU2 <=> LCKE (input pin)
RFU3	RFU3 or LCOM2	CMOS[2]	Reserved for RDIMM and LRDIMM This pins has an alternative function for optional NVDIMM support. • RFU3 <=> LCOM2 (input pin)
Reset output	QRST_n	CMOS[2]	Redriven reset. This is an asynchronous output. It is the responsibility of the DDR4RCD02 QRST_n to reset the DDR4 SDRAM on all DIMM topologies.
Parity outputs	QAPAR QBPAR	CMOS[2]	Redriven parity[3]
Error out	ALERT_n	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs when parity checking is enabled or that the ERROR_IN_n input was asserted, regardless of whether parity checking is enabled or not.

Table 21 — Terminal functions

Signal Group	Signal Name	Type	Description
I^2C Bus pins	SDA	Open drain I/O	I^2C Bus Data
	SCL	CMOS input[4]	I^2C Bus Clock
	SA[2:0]	CMOS input[4]	I^2C Bus Address signals
	BFUNC	CMOS input[5]	Function pin. BFUNC=V_{SS} for primary register, BFUNC=V_{DD} for secondary register
	V_{DDSPD}	Power input	I^2C Bus power input
Miscellaneous pins	VrefCA	$V_{DD}/2$	Input reference voltage for the CMOS inputs.
	V_{DD}	Power Input	Power supply voltage
	V_{SS}	Ground Input	Ground
	AV_{DD}	Analog Power	Analog supply voltage
	AV_{SS}	Analog Ground	Analog ground
	PV_{DD}	Clock Driver Output Power	Clock logic and clock output driver power supply
	PV_{SS}	Clock Driver Output Ground	Clock logic and clock output driver ground
	ZQCAL	Reference	Reference pin for driver calibration
	NU	Mechanical ball	Do not connect on PCB
	RFU[3:0]	I/O	Reserved for future use pins, must be left floating on DIMM and in DDR4RCD02

1. These receivers use internal or external VrefCA as the switching point reference.
2. These outputs with rail to rail signal swing and programmable impedance are optimized for memory applications to drive DRAM inputs over a terminated transmission line.
3. QBPAR will be inverted relative to DPAR if the device is configured with a parity calculation field = 00 in the Parity Control Word.
4. These inputs are 2.5 V inputs
5. This input is a 1.2 V input

Ex. 9 at 61-63 (excerpts for JESD82-31A).

53. On information and belief, the data module of the accused DDR4 LRDIMMs in the second mode is configured to isolate the memory devices from being accessed by the system memory controller. For example, on information and belief, in the second mode, the host-to-DB path is not used to perform read and write operations between the data buffers and the memory devices. *Id.* ("The host-to-DB data path has not been trained at this time so the data that is written to the DRAM comes from the data buffers' internal data control words that are written through the DDR4 register via the BCOM bus."); *see also id.* ("After that the host sends write commands to an arbitrary DRAM location without driving data on the host interface. The data for these write commands come from the DB MPRs.").

54. On information and belief, the data module of the accused DDR4 LRDIMMs in the second mode is configured to transmit one or more second data signals including data patterns provided by the data handler logic elements (i.e. data buffers) to the data ports of the memory devices according to one or more commands output from the control module. For example, the data buffers transmit data signals to and from the data ports of the memory devices during DB-to-DRAM Write Delay mode according to BCW write and read commands (sent from the RCD), respectively:

2.5.3 Control Bus Commands

2.5.3.1 Command List

Table 6 — Data Buffer Control Bus Command Table

Command	Description	BCOM[3:0] Encoding
WR	Write BC4 or BC8 (fixed or on the fly) or BC10 (with CRC enabled) and send accessed rank ID and BL information in the next command time slot, followed by parity in the last command time slot.	1000
RD	Read BC4 or BC8 (fixed or on the fly) and send accessed rank ID and BL information for regular reads or MPR number for MPR override reads in the next command time slot, followed by parity in the last command time slot.	1001
MRS Write	Send MRS Write bits snooped by DDR4 Register and the MRS ID in the following six command time slots, followed by parity in the last command time slot.	1011
BCW Write	Write buffer control word data in the next five command slots, followed by parity in the last command time slot.	1100
BCW Read	Read buffer control word address in the four command slots, followed by parity in the last command time slot.	1101
RFU[1]	Reserved for future use	1110
RFU[1]	Reserved for future use	1111
NOP	Idle, do nothing	1010

1. RFU commands are treated as NOP commands for command sequence error detection

Ex. 9 at 14 (excerpts for JESD82-31A).

2.5.4.4 BCW Write Command

Table 10 shows the sequence for buffer control word write commands.

Table 10 — Multicycle Sequence for BCW Write Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	BCW Write	Buffer control word write access command BCOM[3:0] = 1100
2	DAT0	First data transfer for BCW Write command BCOM[3:0] = {0, DA2, DA1, DA0]
3	DAT1	Second data transfer for BCW Write command BCOM[3:0] = {0, DA5, DA4, DA3}
4	DAT2	Third data transfer for BCW Write command BCOM[3:0] = {0, DA8, DA7, DA6}
5	DAT3	Fourth data transfer for BCW Write command BCOM[3:0] = {0, DA11, DA10, DA9}
6	DAT4	Fifth data transfer for BCW Write command BCOM[3:0] = {0, 0, 0, 0} for Function space 0 BCW writes BCOM[3:0] = {0, 0, 0, 1} for Function space 1 BCW writes BCOM[3:0] = {0, 0, 1, 0} for Function space 2 BCW writes BCOM[3:0] = {0, 0, 1, 1} for Function space 3 BCW writes BCOM[3:0] = {0, 1, 0, 0} for Function space 4 BCW writes BCOM[3:0] = {0, 1, 0, 1} for Function space 5 BCW writes BCOM[3:0] = {0, 1, 1, 0} for Function space 6 BCW writes BCOM[3:0] = {0, 1, 1, 1} for Function space 7 BCW writes
7	PAR[3:0]	Even parity bits for BCW Write command and data PAR[x]: parity bit for 6 previous BCOM[x] transfers
8	Next Cmd	Next Command

The sequence for a BCW Write command is shown in Figure 10 below. The timing diagrams show how the BCW Write command is followed by five data transfer cycles and a parity data transfer cycle. Since the command sequence uses seven cycles it is necessary to include these cycles as part of the tMRD parameter that indicates the spacing from the BCW Write command to the following valid command (also shown in the diagrams).

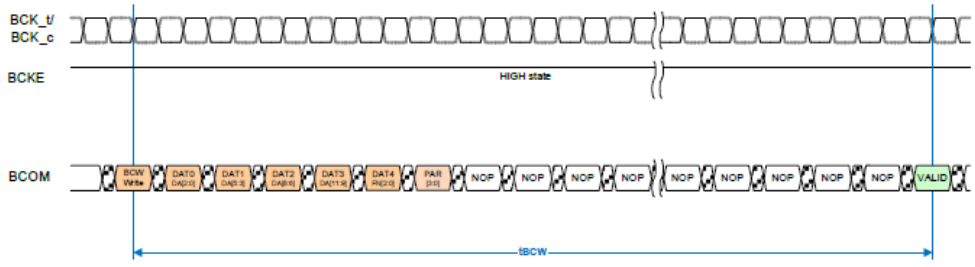


Figure 10 — Buffer Control Word Write command sequence

Ex. 9 at 20-21 (excerpts for JESD82-31A).

2.5.4.5 BCW Read Commands

The DDR4RCD02 generates a BCW Read command on the buffer control bus when it receives a CW Read command in F0RC06 with A12 = 1.

Table 11 shows the sequence for BCW Read commands.

Table 11 — Multicycle Sequence for BCW Read Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	BCW Read	Buffer control word read access command BCOM[3:0] = 1101
2	DAT0	First data transfer for BCW Read command BCOM[3:0] = {0, DA5, DA4, 0}
3	DAT1	Second data transfer for BCW Read command BCOM[3:0] = {0, DA8, DA7, DA6}
4	DAT2	Third data transfer for BCW Read command BCOM[3:0] = {0, DA11, DA10, DA9}
5	DAT3	Fourth data transfer for BCW Read command BCOM[3:0] = {0, 0, 0, 0} for Function space 0 BCW reads BCOM[3:0] = {0, 0, 0, 1} for Function space 1 BCW reads BCOM[3:0] = {0, 0, 1, 0} for Function space 2 BCW reads BCOM[3:0] = {0, 0, 1, 1} for Function space 3 BCW reads BCOM[3:0] = {0, 1, 0, 0} for Function space 4 BCW reads BCOM[3:0] = {0, 1, 0, 1} for Function space 5 BCW reads BCOM[3:0] = {0, 1, 1, 0} for Function space 6 BCW reads BCOM[3:0] = {0, 1, 1, 1} for Function space 7 BCW reads
6	PAR[3:0]	Even parity bits for BCW Read command and data PAR[x]: parity bit for 5 previous BCOM[x] transfers
7	Next Cmd	Next Command

The sequence for BCW Read command is shown in Figure 11 below. The timing diagrams show how the BCW Read command is followed by four data transfer cycles and a parity data transfer cycle. This BCW Read command moves the selected BCW bits to MPR0 and configures the DB for MPR override read mode for the next Read command. The DB treats the first Read command after a BCW Read command as an MPR0 override read (regardless of the BCOM[1:0] bits during the DAT0 cycle of the corresponding BCOM Read command). The read data is driven out after DB_RL(R0) on the host interface DQ pins after the Read command. Just like in regular MPR override read mode, DDR4RCD02 will forward Read command to DRAM but DDR4DB02 will ignore read data from DRAM.

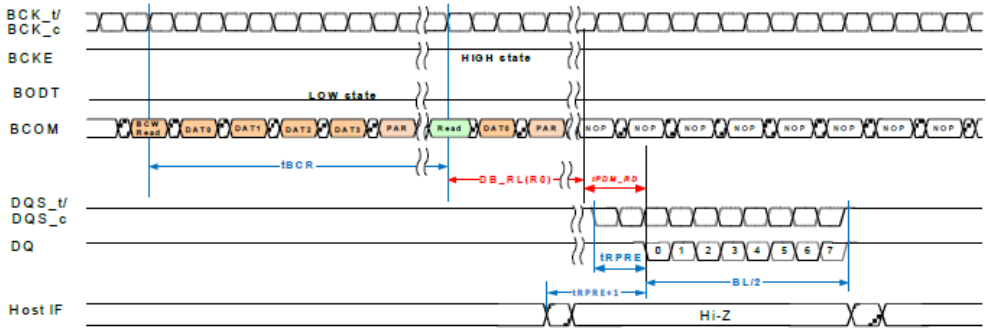


Figure 11 — BCW Read command sequence

Ex. 9 at 22-23 (excerpts for JESD82-31A).

2.20.5 DB-to-DRAM Write Delay (MWD) Training Mode

For the DB-to-DRAM write delay training, the MDQ-MDQS delay adjustments are performed in the data buffer so that the DRAM receives the MDQ and MDQS signals with the optimal phase relationship. The host-to-DB data path has not been trained at this time so the data that is written to the DRAM comes from the data buffer's internal data control words that are written through the DDR4 register via the BCOM bus. Since the DB to DRAM write training requires reading back the data for correctness it is performed after the DRAM to DB read training has already been finished.

To perform DB-to-DRAM write training, the host will first enable the MDQ-MDQS write delay training mode in the Training Mode Control Word (BC0C) and it will also program the MPRs F5BC0x through F5BC3x and F6BC0x through F6BC3x. After that the host sends write commands to an arbitrary DRAM location without driving data on the host interface. The data for these write commands come from the DB MPRs.

MPRx[7:0] is driven to MDQ[7:0], UIx, i.e. the content of MPR0 is driven out first and the content of MPR7 is driven out last.

To check whether the writes were successful, the host reads the data back from the same DRAM location and the data buffer performs a bit wise comparison with the data in the MPRs. If the data pattern is matched, the DQ pins are driven to '1' until the next comparison takes place or until the training mode is disabled. If the data pattern is not matched, the DQ pins are driven to '0'. In addition to driving the DQ pins, status for the MRD training mode is also provided in the Buffer Training Status word (F6BC5x). The status provided in F6BC5x can be modified by the Buffer Training Configuration control word (F6BC4x).

The phase relationship between the DRAM interface data strobe signals (MDQSx_t/MDQSx_c) and their corresponding data signals (MDQx) during write transactions is selected by buffer control words F[3:0]BC8x and F[3:0]BC9x for lower and upper nibble respectively. Since the DDR4DB02 uses the RANK ID fields in the BCOM Write Command and Read Command sequences to select the correct DRAM interface write leveling and DRAM interface receive enable timings for Writes and Reads respectively, the content of BC08 DA[1:0] is don't care while in this training mode. The nominal setting for F[3:0]BC8x/F[3:0]BC9x is one quarter of a cycle delay. The host controller may need to perform additional iterations of the training procedures, including DWL (DRAM Interface Write Leveling) and HWL (Host Interface Write Leveling) when non-default settings are written into F[3:0]BC8x/ F[3:0]BC9x.

For higher DDR4 data rates, fine adjustment of the phase of individual bit lanes relative to MDQS may be required. For this purpose the host controller can utilize the per lane MDQ-MDQS write delay control words F[7:4]BCCx through F[7:4]BCFx. F4BCCx controls the phase of bits MDQ0 and MDQ4 within the lower and upper nibble respectively for Rank 0, F5BCDx controls the phase bits MDQ1 and MDQ5 for Rank 1, and so on. Since all bits within a nibble a generally aligned by routing, only a small range of +/- 3 * 1/64 * t_{CK} is provided for fine-grained adjustment of individual bit lane delay differences. A negative delay in these control words means that the particular data lane requires slightly less delay than the previously established MDQ delay in F[3:0]BC8x or F[3:0]BC9x for the entire nibble. A positive delay in these control words means that the particular data lane requires slightly more delay than the previously established MDQ delay in F[3:0]BC8x or F[3:0]BC9x for the entire nibble.

To exit this training mode, the host controller can go back to resume normal operation or enable other training modes with a BCW to BC0C.

Ex. 6 at 33 (excerpts for JESD82-32A).

55. On information and belief, at least a portion of the memory devices of the accused DDR4 LRDIMMs are configured to receive the one or more second data signals according to the second memory address and control signals from the control module. For example, the RCD sends address and control signals (as part of read and write commands) to the memory devices so that they can receive one or more data signals from the data buffers. *Id.* at 33 (JESD82-32A) ("To

perform DB-to-DRAM write training, the host will first enable the MDQ-MDQS write delay training mode in the Training Mode Control Word (BC0C) and it will also program the MPRs F5BC0x through F5BC3x and F6BC0x through F6BC3x. After that the host sends write commands to an arbitrary DRAM location without driving data on the host interface. The data for these write commands come from the DB MPRs."). Further, the RCD of the accused LRDIMMs sends address and control signals (as part of read and write commands) to the memory devices so that they can receive one or more data signals from the Samsung/Google Data Buffers:

2.20.5 DB-to-DRAM Write Delay (MWD) Training Mode

For the DB-to-DRAM write delay training, the MDQ-MDQS delay adjustments are performed in the data buffer so that the DRAM receives the MDQ and MDQS signals with the optimal phase relationship. The host-to-DB data path has not been trained at this time so the data that is written to the DRAM comes from the data buffer's internal data control words that are written through the DDR4 register via the BCOM bus. Since the DB to DRAM write training requires reading back the data for correctness it is performed after the DRAM to DB read training has already been finished.

To perform DB-to-DRAM write training, the host will first enable the MDQ-MDQS write delay training mode in the Training Mode Control Word (BC0C) and it will also program the MPRs F5BC0x through F5BC3x and F6BC0x through F6BC3x. After that the host sends write commands to an arbitrary DRAM location without driving data on the host interface. The data for these write commands come from the DB MPRs.

MPRx[7:0] is driven to MDQ[7:0], UIx, i.e. the content of MPR0 is driven out first and the content of MPR7 is driven out last.

To check whether the writes were successful, the host reads the data back from the same DRAM location and the data buffer performs a bit wise comparison with the data in the MPRs. If the data pattern is matched, the DQ pins are driven to '1' until the next comparison takes place or until the training mode is disabled. If the data pattern is not matched, the DQ pins are driven to '0'. In addition to driving the DQ pins, status for the MRD training mode is also provided in the Buffer Training Status word (F6BC5x). The status provided in F6BC5x can be modified by the Buffer Training Configuration control word (F6BC4x).

The phase relationship between the DRAM interface data strobe signals (MDQSx_t/MDQSx_c) and their corresponding data signals (MDQx) during write transactions is selected by buffer control words F[3:0]BC8x and F[3:0]BC9x for lower and upper nibble respectively. Since the DDR4DB02 uses the RANK ID fields in the BCOM Write Command and Read Command sequences to select the correct DRAM interface write leveling and DRAM interface receive enable timings for Writes and Reads respectively, the content of BC08 DA[1:0] is don't care while in this training mode. The nominal setting for F[3:0]BC8x/F[3:0]BC9x is one quarter of a cycle delay. The host controller may need to perform additional iterations of the training procedures, including DWL (DRAM Interface Write Leveling) and HWL (Host Interface Write Leveling) when non-default settings are written into F[3:0]BC8x/ F[3:0]BC9x.

For higher DDR4 data rates, fine adjustment of the phase of individual bit lanes relative to MDQS may be required. For this purpose the host controller can utilize the per lane MDQ-MDQS write delay control words F[7:4]BCCx through F[7:4]BCFx. F4BCCx controls the phase of bits MDQ0 and MDQ4 within the lower and upper nibble respectively for Rank 0, F5BCDx controls the phase bits MDQ1 and MDQ5 for Rank 1, and so on. Since all bits within a nibble a generally aligned by routing, only a small range of +/- 3 * 1/64 * t_{CK} is provided for fine-grained adjustment of individual bit lane delay differences. A negative delay in these control words means that the particular data lane requires slightly less delay than the previously established MDQ delay in F[3:0]BC8x or F[3:0]BC9x for the entire nibble. A positive delay in these control words means that the particular data lane requires slightly more delay than the previously established MDQ delay in F[3:0]BC8x or F[3:0]BC9x for the entire nibble.

To exit this training mode, the host controller can go back to resume normal operation or enable other training modes with a BCW to BC0C.

Ex. 6 at 33 (excerpts for JESD82-32A).

56. On information and belief, Samsung and Google also each indirectly infringes the '523 patent, as provided in 35 U.S.C. § 271(b), by inducing infringement by others, such as Samsung's and Google's customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung and Google each has induced, and currently induces, the infringement of the '523 patent through its affirmative acts of making, selling, offering to sell, distributing, and/or otherwise making available the accused DDR4 LRDIMM and other materially similar products that infringe the '523 Patent. On information and belief, Samsung and Google each provides specifications, datasheets, instruction manuals, and/or other materials that encourage and facilitate infringing use of the accused DDR4 LRDIMM products and other materially similar products by users in a manner that it knows or should have known would result in infringement and with the intent of inducing infringement.

57. On information and belief, Samsung and Google also each indirectly infringes the '523 patent, as provided in 35 U.S.C. § 271(c), contributing to direct infringement committed by others, such as customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung and Google each contributed to, and currently contributes to, Samsung's and Google's customers' and end users' infringement of the '523 patent through their affirmative acts of selling and offering to sell, in this District and elsewhere in the United States, the accused DDR4 LRDIMM and other materially similar products/services that infringe the '523 patent. On information and belief, the accused DDR4 LRDIMM products and other materially similar products/services have no substantial noninfringing use and constitute a material part of the patented invention. On information and belief, Samsung and Google are aware that the product or process that includes the accused DDR4 LRDIMM and other materially similar products would be covered by one or more claims of the '523 patent. On information and belief,

the use of the product or process that includes the accused DDR4 LRDIMM and other materially similar products infringes at least one claim of the '523 patent.

58. Samsung's and Google's infringement of the '523 patent has damaged and will continue to damage Netlist.

59. On information and belief, Samsung has had actual notice of the '523 patent since at least October 15, 2020. Samsung's infringement of the '523 patent has been continuing and willful. Samsung continues to commit acts of infringement despite a high likelihood that its actions constitute infringement, and Samsung knew or should have known that its actions constituted an unjustifiably high risk of infringement.

60. On information and belief, Google has had actual notice of the '523 patent since at least October 15, 2021, when Samsung initiated this instant declaratory judgment action. Google continues to commit acts of infringement despite a high likelihood that its actions constitute infringement, and Google knew or should have known that its actions constituted an unjustifiably high risk of infringement.

Count II
(Infringement of the '595 Patent)

61. Netlist alleges and incorporates by reference the allegations of the preceding paragraphs of the Affirmative Defenses, Counterclaims, and Cross-claims as if fully set forth herein.

62. On information and belief, Samsung and Google each directly infringed and is currently infringing at least one claim of the '595 patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the Accused Instrumentalities. For example, and as shown below, the Accused Instrumentalities infringe at least claim 1 of the '595 patent.

63. To the extent the preamble is limiting, on information and belief, each Accused Instrumentalities comprises a memory module operable with a memory controller of a host system. For example, Samsung's website markets and contains datasheets for the accused DDR4 RDIMMs:

Registered DIMM

Include a register for enhancing clock, command and control signals
Error correction available by added 8 bit parity signals
Supports x4 / x8 Organization / up to 2 ranks per DIMM and 3DPC configuration
Application : Server

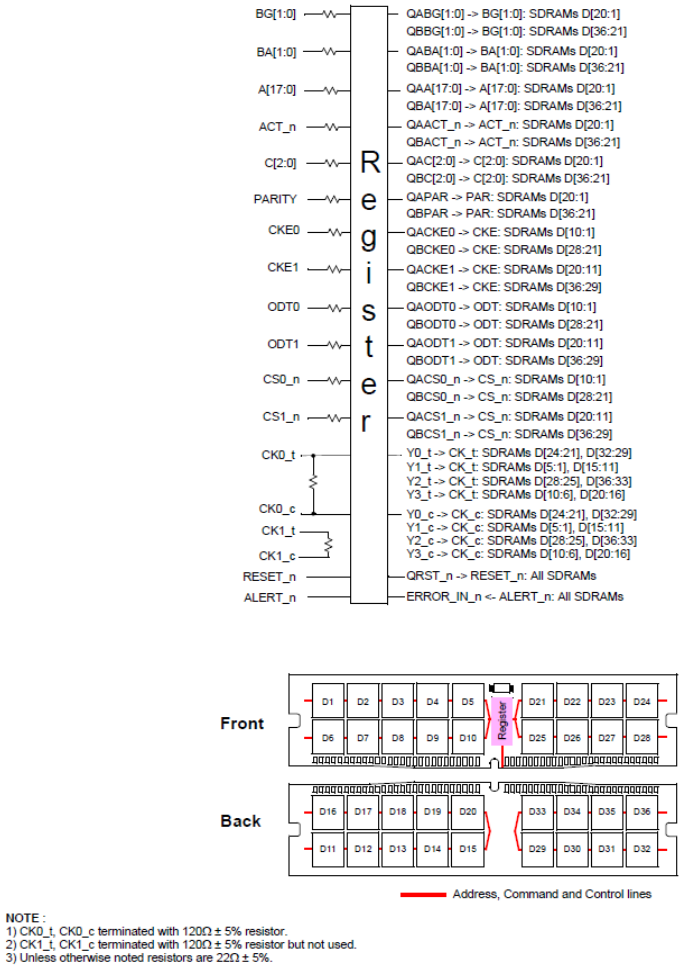
Ex. 7 (depiction of a Samsung DDR4 RDIMM, M393AAG40M32).

64. On information and belief, the Accused Instrumentalities each comprise a printed circuit board (PCB) having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller. The edge connections include first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections. For example, the datasheet of M393AAG40M32 shows the first edge connections, the second edge connections, and the error edge connection.

9. FUNCTION BLOCK DIAGRAM:

9.1 128GB, 16Gx72 Module

9.1.1 (PC4-RDIMM Populated as 2 physical ranks / 2 logical ranks of x4 DDR4 SDRAMs)



NOTE :
1) CK0_t, CK0_c terminated with 120Ω ± 5% resistor.
2) CK1_t, CK1_c terminated with 120Ω ± 5% resistor but not used.
3) Unless otherwise noted resistors are 22Ω ± 5%.

Ex. 8 at 12 (Datasheet for M393AAG40M32).

5. PIN DESCRIPTION

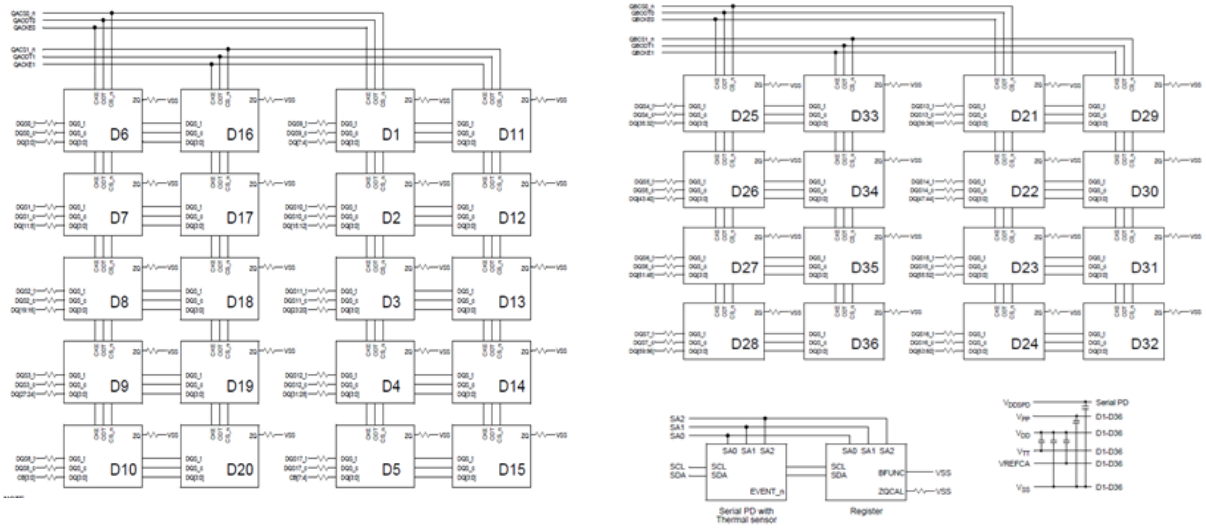
Pin Name	Description
A0-A17[1)]	Register address input
BA0, BA1	Register bank select input
BG0, BG1	Register bank group select input
RAS_n[2)]	Register row address strobe input
CAS_n[3)]	Register column address strobe input
WE_n[4)]	Register write enable input
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input
CKE0, CKE1	Register clock enable lines input
ODT0, ODT1	Register on-die termination control lines input
ACT_n	Register input for activate input
DQ0–DQ63	DIMM memory data bus
CB0–CB7	DIMM ECC check bits
DQS0_t-DQS17_t	Data Buffer data strobes (positive line of differential pair)
DQS0_c-DQS17_c	Data Buffer data strobes (negative line of differential pair)
CK0_t, CK1_t	Register clock input (positive line of differential pair)
CK0_c, CK1_c	Register clocks input (negative line of differential pair)

Pin Name	Description
SCL	I2C serial bus clock for SPD/TS and register
SDA	I2C serial bus data line for SPD/TS and register
SA0-SA2	I2C slave address select for SPD/TS and register
PAR	Register parity input
VDD	SDRAM core power supply
VPP	SDRAM activating power supply
VREFCA	SDRAM command/address reference supply
VSS	Power supply return (ground)
VDDSPD	Serial SPD/TS positive power supply
ALERT_n	Register ALERT_n output
RESET_n	Set Register and SDRAMs to a Known State
EVENT_n	SPD signals a thermal event has occurred
VTT	SDRAM I/O termination supply
RFU	Reserved for future use

NOTE :
1) Address A17 is only valid for 16 Gb x4 based SDRAMs.
2) RAS_n is a multiplexed function with A16.
3) CAS_n is a multiplexed function with A15.
4) WE_n is a multiplexed function with A14.

Id. at 5.

65. On information and belief, the Accused Instrumentalities each comprise a dynamic random access memory (DRAM) elements on the printed circuit board. For example, the datasheet provides the function block diagrams including the DRAM elements on the printed circuit board:



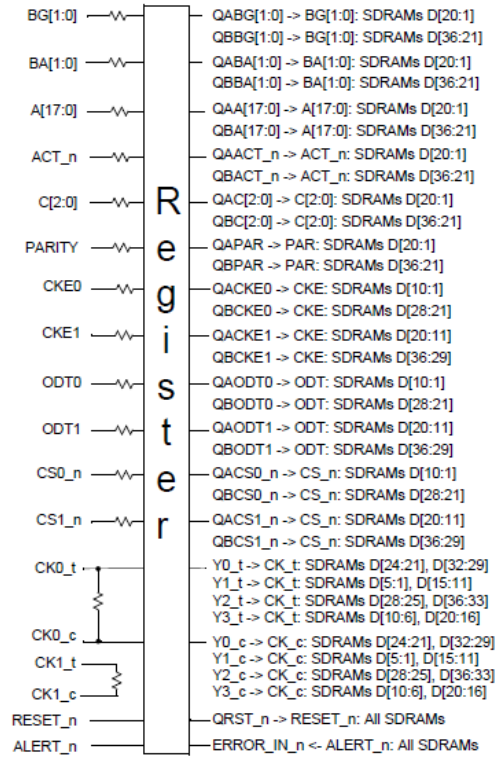
Ex. 8 at 13-14 (M393AAG40M32datasheet) (SDRAM devices D1, D2 . . . D. 35, D. 36).

66. On information and belief, the Accused Instrumentalities each includes a module controller on the PCB and coupled to the DRAM elements. For example,

9. FUNCTION BLOCK DIAGRAM:

9.1 128GB, 16Gx72 Module

9.1.1 (PC4-RDIMM Populated as 2 physical ranks / 2 logical ranks of x4 DDR4 SDRAMs)



NOTE :
1) CK0_t, CK0_c terminated with 120Ω ± 5% resistor.
2) CK1_t, CK1_c terminated with 120Ω ± 5% resistor but not used.
3) Unless otherwise noted resistors are 22Ω ± 5%.

Ex. 8 at 12 (M393AAG40M32 datasheet) (showing the register and "ALERT_n"/"ERROR_In_n).

5. PIN DESCRIPTION

Pin Name	Description
A0-A17[1)]	Register address input
BA0, BA1	Register bank select input
BG0, BG1	Register bank group select input
RAS_n[2)]	Register row address strobe input
CAS_n[3)]	Register column address strobe input
WE_n[4)]	Register write enable input
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input
CKE0, CKE1	Register clock enable lines input
ODT0, ODT1	Register on-die termination control lines input
ACT_n	Register input for activate input
DQ0–DQ63	DIMM memory data bus
CB0–CB7	DIMM ECC check bits
DQS0_t-DQS17_t	Data Buffer data strobes (positive line of differential pair)
DQS0_c-DQS17_c	Data Buffer data strobes (negative line of differential pair)
CK0_t, CK1_t	Register clock input (positive line of differential pair)
CK0_c, CK1_c	Register clocks input (negative line of differential pair)

Pin Name	Description
SCL	I2C serial bus clock for SPD/TS and register
SDA	I2C serial bus data line for SPD/TS and register
SA0-SA2	I2C slave address select for SPD/TS and register
PAR	Register parity input
VDD	SDRAM core power supply
VPP	SDRAM activating power supply
VREFCA	SDRAM command/address reference supply
VSS	Power supply return (ground)
VDDSPD	Serial SPD/TS positive power supply
ALERT_n	Register ALERT_n output
RESET_n	Set Register and SDRAMs to a Known State
EVENT_n	SPD signals a thermal event has occurred
VTT	SDRAM I/O termination supply
RFU	Reserved for future use

NOTE :
1) Address A17 is only valid for 16 Gb x4 based SDRAMs.
2) RAS_n is a multiplexed function with A16.
3) CAS_n is a multiplexed function with A15.
4) WE_n is a multiplexed function with A14.

Ex. 8 at 7 (M393AAG40M32 datasheets).

67. Further, the module controller of the Accused Instrumentalities has an open drain output coupled to the error edge connection. For example, the RCD contains an ALERT_n pin, which is an open drain output coupled to the error edge connection of the PCB.

68. On information and belief, the Accused Instrumentalities each contains an RCD that is configurable to operate in a first mode (e.g. a normal operating mode) and a second mode (e.g. the Clock-to-CA training mode).

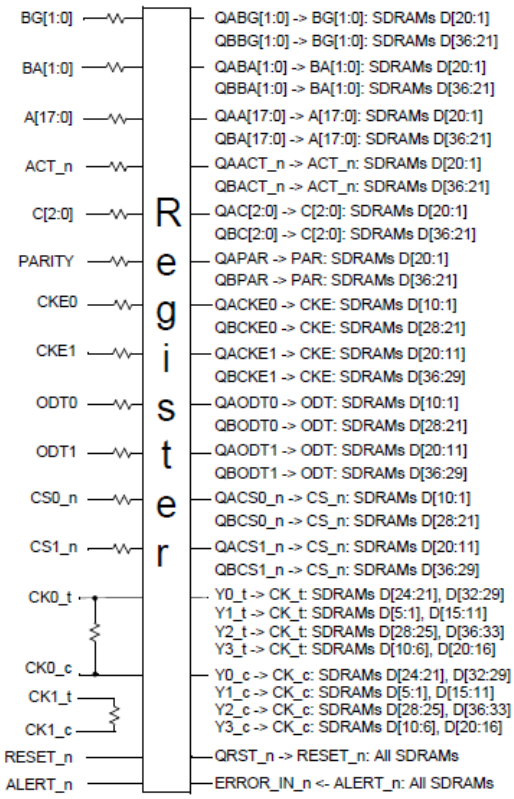
69. On information and belief, the Accused Instrumentalities in the first mode (the normal operating mode) are configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections. For example, during the first mode, the RCD of the Accused Instrumentalities receives address and control signals corresponding to read and write commands from the memory controller via the second edge connections. The RCD

outputs corresponding address and control signals to the SDRAM devices, which cause the SDRAM devices to execute read and write operations:

9. FUNCTION BLOCK DIAGRAM:

9.1 128GB, 16Gx72 Module

9.1.1 (PC4-RDIMM Populated as 2 physical ranks / 2 logical ranks of x4 DDR4 SDRAMs)



NOTE :
1) CK0_t, CK0_c terminated with 120Ω ± 5% resistor.
2) CK1_t, CK1_c terminated with 120Ω ± 5% resistor but not used.
3) Unless otherwise noted resistors are 22Ω ± 5%.

Ex. 8 at 12 (M393AAG40M32).

70. On information and belief, the Accused Instrumentalities in the second mode (clock-to-CA training mode) are not accessed by the memory controller for normal memory read or write operations because the DRAMs under the second mode are isolated from normal use, and normal operational read/write commands are not decoded.

71. On information and belief, the Accused Instrumentalities in the second mode are configurable to perform operations related to one or more training sequences.

72. On information and belief, while the Accused Instrumentalities are in the first mode, the memory controller (RCD) is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations. For example, during the first mode, the RCD receives address and control signals corresponding to read and write commands from the memory controller via the second edge connections.

73. Further, in the first mode, the SDRAM elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals. For example, the RCD outputs the address and control signals to the SDRAM devices, which cause the SDRAM devices to execute read and write operations. The SDRAM components receive these registered C/A signals from the RCD and in accordance, output data to the host in a read operation or receive data from the host in a write operation via the first edge (data) connections.

74. The module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the Accused Instrumentalities are in the first mode. For example, the ALERT_n pin of the Accused Instrumentalities is configurable to indicate a parity error while the memory module operates in the first mode (e.g., a normal mode of operation).

5. PIN DESCRIPTION

Pin Name	Description
A0-A17[1)]	Register address input
BA0, BA1	Register bank select input
BG0, BG1	Register bank group select input
RAS_n[2)]	Register row address strobe input
CAS_n[3)]	Register column address strobe input
WE_n[4)]	Register write enable input
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input
CKE0, CKE1	Register clock enable lines input
ODT0, ODT1	Register on-die termination control lines input
ACT_n	Register input for activate input
DQ0–DQ63	DIMM memory data bus
CB0–CB7	DIMM ECC check bits
DQS0_t-DQS17_t	Data Buffer data strobes (positive line of differential pair)
DQS0_c-DQS17_c	Data Buffer data strobes (negative line of differential pair)
CK0_t, CK1_t	Register clock input (positive line of differential pair)
CK0_c, CK1_c	Register clocks input (negative line of differential pair)

Pin Name	Description
SCL	I2C serial bus clock for SPD/TS and register
SDA	I2C serial bus data line for SPD/TS and register
SA0-SA2	I2C slave address select for SPD/TS and register
PAR	Register parity input
VDD	SDRAM core power supply
VPP	SDRAM activating power supply
VREFCA	SDRAM command/address reference supply
VSS	Power supply return (ground)
VDDSPD	Serial SPD/TS positive power supply
ALERT_n	Register ALERT_n output
RESET_n	Set Register and SDRAMs to a Known State
EVENT_n	SPD signals a thermal event has occurred
VTT	SDRAM I/O termination supply
RFU	Reserved for future use

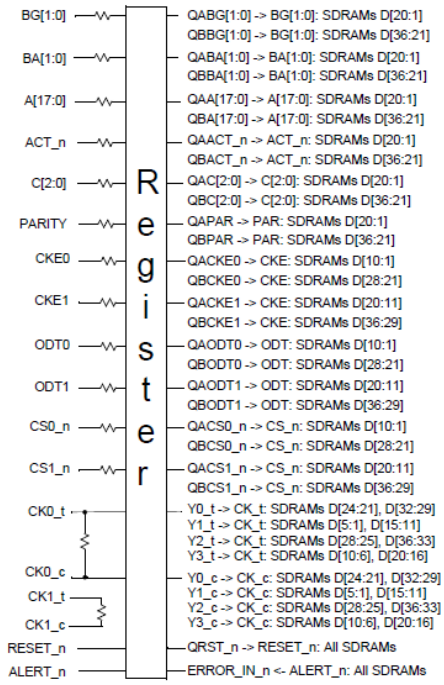
NOTE :
1) Address A17 is only valid for 16 Gb x4 based SDRAMs.
2) RAS_n is a multiplexed function with A16.
3) CAS_n is a multiplexed function with A15.
4) WE_n is a multiplexed function with A14.

Ex. 8 at 7 (M393AAG40M32 datasheet).

9. FUNCTION BLOCK DIAGRAM:

9.1 128GB, 16Gx72 Module

9.1.1 (PC4-RDIMM Populated as 2 physical ranks / 2 logical ranks of x4 DDR4 SDRAMs)



NOTE :
1) CK0_t, CK0_c terminated with 120Ω ± 5% resistor.
2) CK1_t, CK1_c terminated with 120Ω ± 5% resistor but not used.
3) Unless otherwise noted resistors are 22Ω ± 5%.

Ex. 8 at 12 (M393AAG40M32).

75. On information and belief, in the second mode, the Accused Instrumentalities each contains a module controller which is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection to a first state or to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.

76. On information and belief, Samsung and Google each also indirectly infringes the '595 patent, as provided in 35 U.S.C. § 271(b), by inducing infringement by others, such as their customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung and Google each has induced, and currently induces, the infringement of the '595 patent through their affirmative acts of making, selling, offering to sell, distributing, and/or otherwise making available the Accused Instrumentalities that infringe the '595 patent. On information and belief, Samsung and Google each provides specifications, datasheets, instruction manuals, and/or other materials that encourage and facilitate infringing use of the Accused Instrumentalities by users in a manner that it knows or should have known would result in infringement and with the intent of inducing infringement.

77. On information and belief, Samsung and Google each indirectly infringes the '595 patent, as provided in 35 U.S.C. § 271(c), contributing to direct infringement committed by others, such as customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung and Google each contributed to, and currently contributes to, their customers' and end users' infringement of the '595 patent through its affirmative acts of selling and offering to sell, in this District and elsewhere in the United States, the Accused Instrumentalities that infringe the '595 patent. On information and belief, the Accused Instrumentalities have no substantial noninfringing use and constitute a material part of the patented invention. On information and belief, Samsung and Google are aware that the product or process that includes the Accused Instrumentalities would be covered by one or more claims of the '595 patent. On information and belief, the use of the product or process that includes the Accused Instrumentalities infringes at least one claim of the '595 patent.

78. Samsung's and Google's infringement of the '595 patent has damaged and will continue to damage Netlist.

79. Samsung has had actual notice of the '595 patent since at least October 15, 2020. Samsung's infringement of the '595 patent has been continuing and willful. Samsung continues to commit acts of infringement despite a high likelihood that its actions constitute infringement, and Samsung knew or should have known that its actions constituted an unjustifiably high risk of infringement.

80. On information and belief, Google has had actual notice of the '595 patent since at least October 15, 2021, when Samsung initiated this instant declaratory judgment action. Google continues to commit acts of infringement despite a high likelihood that its actions constitute infringement, and Google knew or should have known that its actions constituted an unjustifiably high risk of infringement.

Count III
(Infringement of the '218 Patent)

81. Netlist alleges and incorporates by reference the allegations of the preceding paragraphs of the Affirmative Defenses, Counterclaims, and Cross-claims as if fully set forth herein.

82. On information and belief, Samsung and Google each directly infringed and is currently infringing at least one claim of the '218 patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the Accused Instrumentalities. For example, and as shown below, the Accused Instrumentalities infringe at least claim 1 of the '218 patent.

83. To the extent the preamble is limiting, on information and belief, each Accused Instrumentalities comprises a memory module operable with a memory controller of a host system.

For example, Samsung's website markets and contains datasheets for the accused DDR4 RDIMMs:

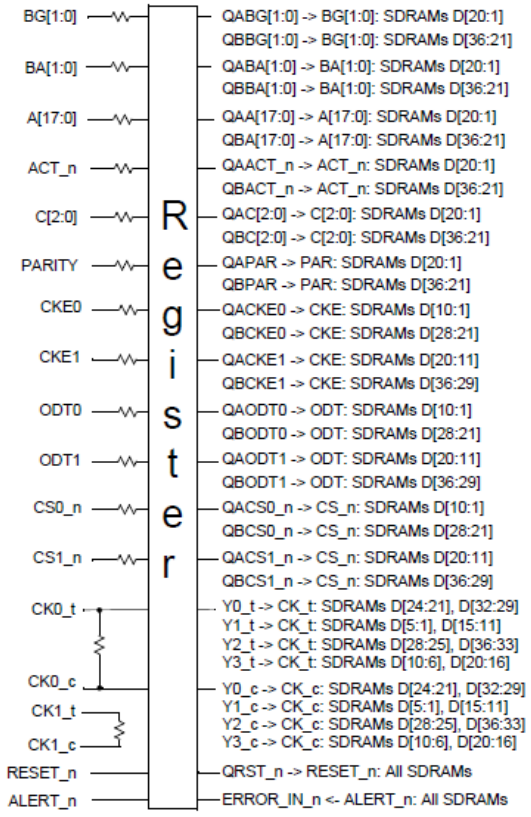
Ex. 7 (depiction of a Samsung DDR4 RDIMM, M393AAG40M32).

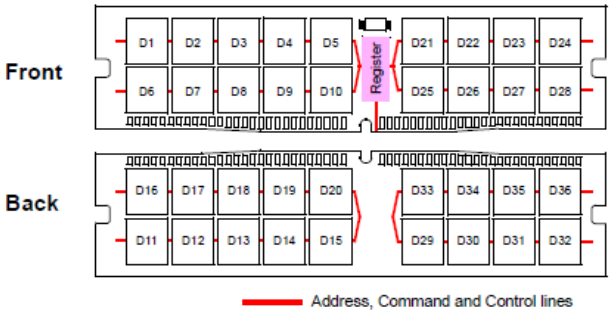
84. On information and belief, the Accused Instrumentalities each comprise a printed circuit board (PCB) having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller. The edge connections include first edge connections, second edge connections, and an error edge connection.

9. FUNCTION BLOCK DIAGRAM:

9.1 128GB, 16Gx72 Module

9.1.1 (PC4-RDIMM Populated as 2 physical ranks / 2 logical ranks of x4 DDR4 SDRAMs)

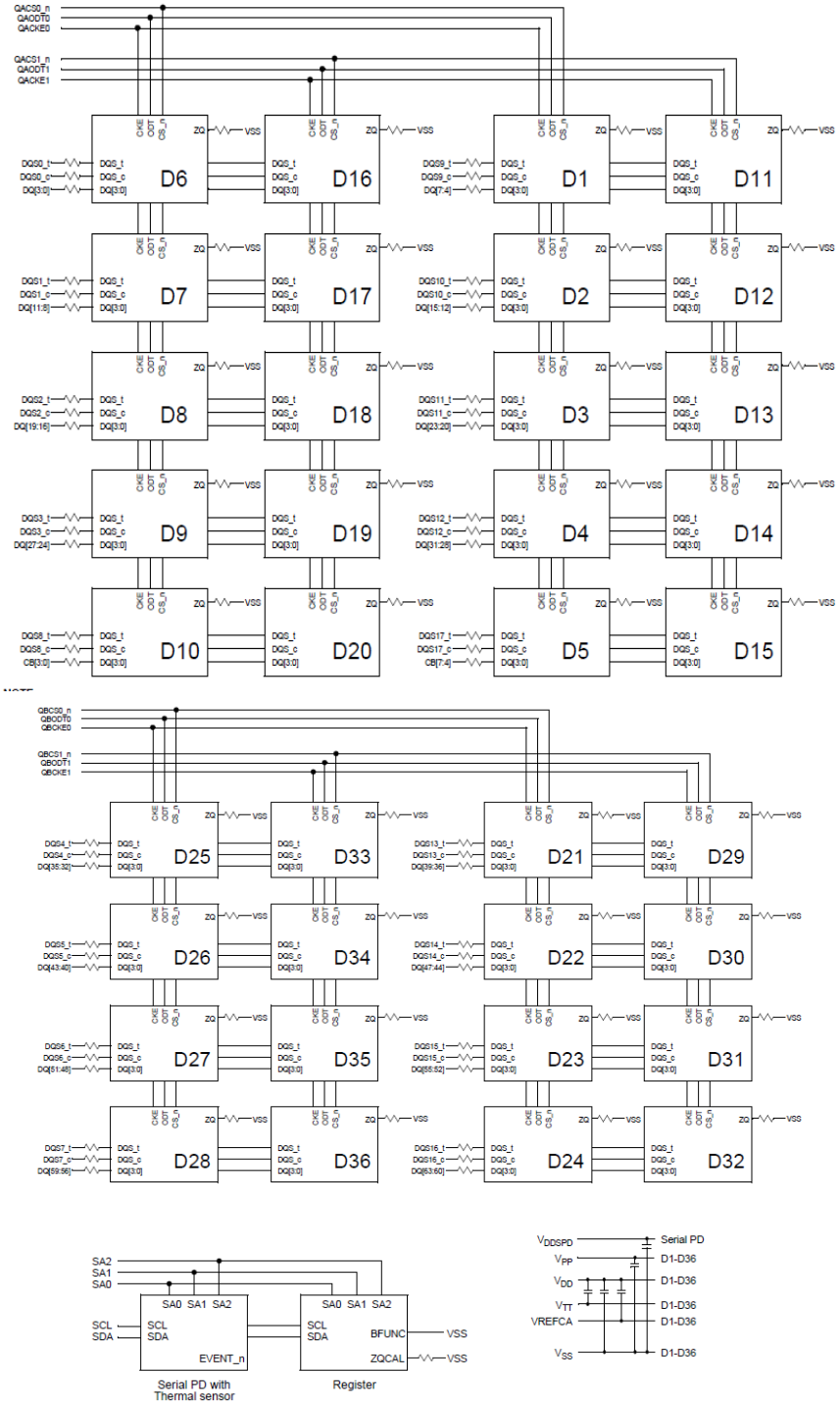




NOTE :
1) CK0_t, CK0_c terminated with 120Ω ± 5% resistor.
2) CK1_t, CK1_c terminated with 120Ω ± 5% resistor but not used.
3) Unless otherwise noted resistors are 22Ω ± 5%.

Ex. 8 at 12 (Datasheet for M393AAG40M32).

85. On information and belief, the Accused Instrumentalities each comprise a dynamic random access memory (DRAM) elements on the printed circuit board. For example, the datasheet provides the function block diagrams including the DRAM elements on the printed circuit board:



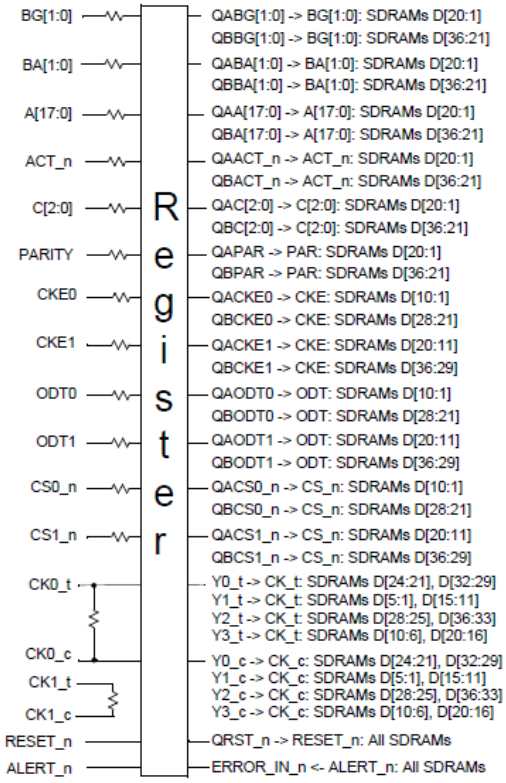
Ex. 8 at 13-14 (M393AAG40M32datasheet) (SDRAM devices D1, D2 . . . D. 35, D. 36).

86. On information and belief, the Accused Instrumentalities each includes a module controller on the PCB and coupled to the DRAM elements. The module controller has an open drain output coupled to the error edge connection. For example,

9. FUNCTION BLOCK DIAGRAM:

9.1 128GB, 16Gx72 Module

9.1.1 (PC4-RDIMM Populated as 2 physical ranks / 2 logical ranks of x4 DDR4 SDRAMs)



NOTE :
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2) CK1_t, CK1_c terminated with 120Ω ± 5% resistor but not used.
3) Unless otherwise noted resistors are 22Ω ± 5%.

Ex. 8 at 12 (M393AAG40M32) (showing the register and "ALERT_n"/"ERROR_In_n).

5. PIN DESCRIPTION

Pin Name	Description
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WE_n[4)]	Register write enable input
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input
CKE0, CKE1	Register clock enable lines input
ODT0, ODT1	Register on-die termination control lines input
ACT_n	Register input for activate input
DQ0–DQ63	DIMM memory data bus
CB0–CB7	DIMM ECC check bits
DQS0_t-DQS17_t	Data Buffer data strobes (positive line of differential pair)
DQS0_c-DQS17_c	Data Buffer data strobes (negative line of differential pair)
CK0_t, CK1_t	Register clock input (positive line of differential pair)
CK0_c, CK1_c	Register clocks input (negative line of differential pair)

Pin Name	Description
SCL	I2C serial bus clock for SPD/TS and register
SDA	I2C serial bus data line for SPD/TS and register
SA0-SA2	I2C slave address select for SPD/TS and register
PAR	Register parity input
VDD	SDRAM core power supply
VPP	SDRAM activating power supply
VREFCA	SDRAM command/address reference supply
VSS	Power supply return (ground)
VDDSPD	Serial SPD/TS positive power supply
ALERT_n	Register ALERT_n output
RESET_n	Set Register and SDRAMs to a Known State
EVENT_n	SPD signals a thermal event has occurred
VTT	SDRAM I/O termination supply
RFU	Reserved for future use

NOTE :
1) Address A17 is only valid for 16 Gb x4 based SDRAMs.
2) RAS_n is a multiplexed function with A16.
3) CAS_n is a multiplexed function with A15.
4) WE_n is a multiplexed function with A14.

Ex. 8 at 7 (M393AAG40M32).

87. On information and belief, the Accused Instrumentalities each contains an RCD that is operable under a first mode (i.e. Clock-to-CA training mode) and a second mode (i.e. normal operating mode).

88. On information and belief, the Accused Instrumentalities in the first mode (Clock-to-CA mode) are configured to be trained with one or more training sequences.

89. On information and belief, the Accused Instrumentalities in the second mode (the normal operation mode) are configured to perform one or more memory read or write operations.

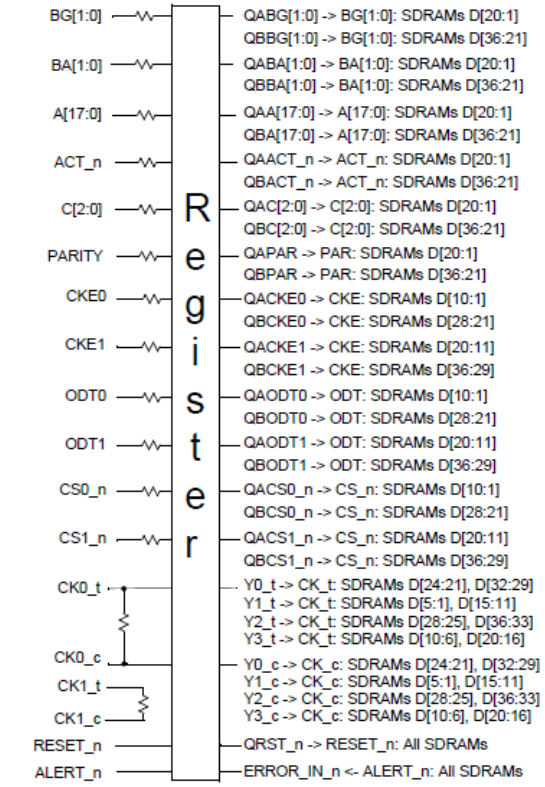
90. Further, when the Accused Instrumentalities are under the second mode, the memory read or write operations by communicating data signals via the first edge connections in response to address and command signals received via the second edge connections. For example, during the second mode (e.g., a normal mode of operation), the RCD receives address and control

signals corresponding to read and write commands from the memory controller via the second edge connections. The RCD outputs corresponding address and control signals to the SDRAM devices, which cause the SDRAM devices to execute read and write operations.

9. FUNCTION BLOCK DIAGRAM:

9.1 128GB, 16Gx72 Module

9.1.1 (PC4-RDIMM Populated as 2 physical ranks / 2 logical ranks of x4 DDR4 SDRAMs)



NOTE :
1) CK0_t, CK0_c terminated with 120Ω ± 5% resistor.
2) CK1_t, CK1_c terminated with 120Ω ± 5% resistor but not used.
3) Unless otherwise noted resistors are 22Ω ± 5%.

Ex. 8 at 12 (M393AAG40M32 datasheet).

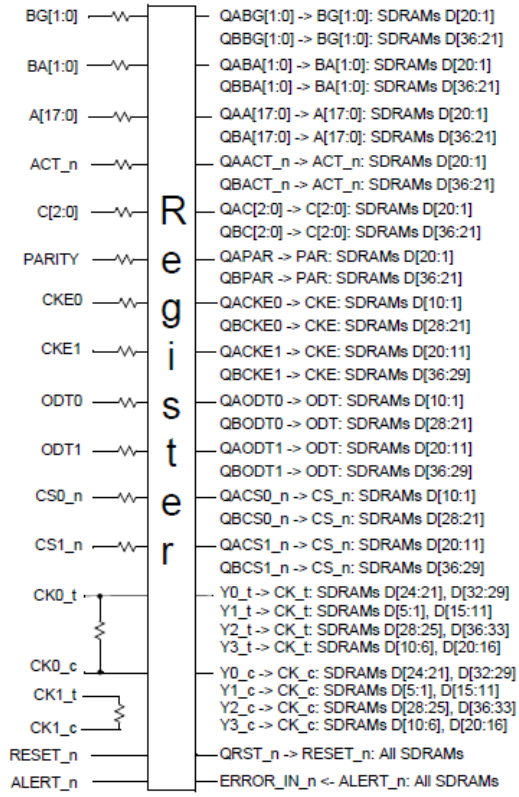
91. These memory read or write operations under the second mode are not associated with the one or more training sequences. For example, while the Accused Instrumentalities are in Clock-to-CA training mode (e.g., a first mode), the dynamic random access memory devices (DRAMs) of the memory module are isolated from normal use, and normal operational read/write commands are not decoded.

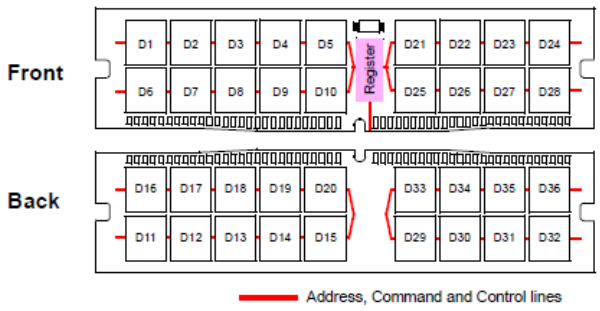
92. On information and belief, while the Accused Instrumentalities are under the second mode (the normal operation mode), the module controller (the RCD) is configured to receive via the second edge connections the address and command signals associated with the one or more memory read or write operations and to control the dynamic random access memory elements in accordance with the address and command signals. For example, while the memory module is in a second mode (e.g., a normal mode of operation), the RCD receives address and control signals corresponding to read and write commands via the second edge connections. The RCD outputs corresponding address and control signals to the SDRAM devices, which cause the SDRAM devices to execute read and write operations.

9. FUNCTION BLOCK DIAGRAM:

9.1 128GB, 16Gx72 Module

9.1.1 (PC4-RDIMM Populated as 2 physical ranks / 2 logical ranks of x4 DDR4 SDRAMs)





NOTE :
1) CK0_t, CK0_c terminated with 120Ω ± 5% resistor.
2) CK1_t, CK1_c terminated with 120Ω ± 5% resistor but not used.
3) Unless otherwise noted resistors are 22Ω ± 5%.

Ex. 8 at 12 (M393AAG40M32 datasheet).

93. On information and belief, while the Accused Instrumentalities are in the second mode (the normal operation mode), the module controller (the RCD) is configured to output via the open drain output and the error edge connection a signal indicating a parity error having occurred. For example, the ALERT_n pin of the Accused Instrumentalities is configurable for indicating a parity error while the memory module operates in the first mode (e.g., a normal mode of operation).

5. PIN DESCRIPTION

Pin Name	Description
A0-A17[1)]	Register address input
BA0, BA1	Register bank select input
BG0, BG1	Register bank group select input
RAS_n[2)]	Register row address strobe input
CAS_n[3)]	Register column address strobe input
WE_n[4)]	Register write enable input
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input
CKE0, CKE1	Register clock enable lines input
ODT0, ODT1	Register on-die termination control lines input
ACT_n	Register input for activate input
DQ0–DQ63	DIMM memory data bus
CB0–CB7	DIMM ECC check bits
DQS0_t-DQS17_t	Data Buffer data strobes (positive line of differential pair)
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Pin Name	Description
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NOTE :
1) Address A17 is only valid for 16 Gb x4 based SDRAMs.
2) RAS_n is a multiplexed function with A16.
3) CAS_n is a multiplexed function with A15.
4) WE_n is a multiplexed function with A14.

Ex. 8 at 7 (M393AAG40M32 datasheet).

94. On information and belief, while the Accused Instrumentalities are in the first mode, the module controller (RCD) is configured to drive a notification signal associated with the one or more training sequences to the error edge connection via the open drain output.

95. On information and belief, Samsung and Google each also indirectly infringes the '218 patent, as provided in 35 U.S.C. § 271(b), by inducing infringement by others, such as their customers and end users, in this District and elsewhere in the United States. For example, on

information and belief, Samsung and Google each has induced, and currently induces, the infringement of the '218 patent through their affirmative acts of making, selling, offering to sell, distributing, and/or otherwise making available the Accused Instrumentalities that infringe the '218 patent. On information and belief, Samsung and Google each provides specifications, datasheets, instruction manuals, and/or other materials that encourage and facilitate infringing use of the Accused Instrumentalities by users in a manner that it knows or should have known would result in infringement and with the intent of inducing infringement.

96. On information and belief, Samsung and Google each indirectly infringes the '218 patent, as provided in 35 U.S.C. § 271(c), contributing to direct infringement committed by others, such as customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung and Google each contributed to, and currently contributes to, their customers' and end users' infringement of the '218 patent through its affirmative acts of selling and offering to sell, in this District and elsewhere in the United States, the Accused Instrumentalities that infringe the '218 patent. On information and belief, the Accused Instrumentalities have no substantial noninfringing use and constitute a material part of the patented invention. On information and belief, Samsung and Google are aware that the product or process that includes the Accused Instrumentalities would be covered by one or more claims of the '218 patent. On information and belief, the use of the product or process that includes the Accused Instrumentalities infringes at least one claim of the '218 patent.

97. Samsung's and Google's infringement of the '218 patent has damaged and will continue to damage Netlist.

98. Samsung has had actual notice of the '218 patent since at least October 15, 2020. Samsung's infringement of the '218 patent has been continuing and willful. Samsung continues

to commit acts of infringement despite a high likelihood that its actions constitute infringement, and Samsung knew or should have known that its actions constituted an unjustifiably high risk of infringement.

99. On information and belief, Google has had actual notice of the '218 patent since at least October 15, 2021, when Samsung initiated this instant declaratory judgment action. Google continues to commit acts of infringement despite a high likelihood that its actions constitute infringement, and Google knew or should have known that its actions constituted an unjustifiably high risk of infringement.

DEMAND FOR TRIAL BY JURY

100. Pursuant to Federal Rule of Civil Procedure 38(b), Netlist hereby demands a trial by jury on all issues triable to a jury.

PRAYER FOR RELIEF

101. WHEREFORE, Netlist respectfully requests that this Court enter judgment in Netlist's favor, ordering, finding, declaring, and/or awarding Netlist relief as follows:

a. that Samsung and Google each infringes the Patents-in-Suit;

b. all equitable relief the Court deems just and proper as a result of Samsung's and Google's infringement;

c. an award of damages resulting from Samsung's and Google's acts of infringement in accordance with 35 U.S.C. § 284;

d. that Samsung's and Google's infringement of the Patents-in-Suit is willful;

e. enhanced damages pursuant to 35 U.S.C. § 284;

f. that this is an exceptional case and awarding Netlist its reasonable attorneys' fees pursuant to 35 U.S.C. § 285;

g. an accounting for acts of infringement and supplemental damages, without limitation, prejudgment and post-judgment interest; and

h. such other equitable relief which may be requested and to which Netlist is entitled.

/s/ Emily S. DiBenedetto

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Dated: September 12, 2022